EXHIBIT 40

SEALED DOCUMENT

EXHIBIT 41

1980-1989

- History of Kodak
  - George Eastman
  - Building the Foundation
  - Broadening the Impact of Pictures
  - Transforming for the Future
  - Imaging- the basics
  - Quality and Ethics
  - Milestones- chronology
    - 1878-1929
    - 1930-1959
    - 1960-1979
    - ▶ **1980-1989**
    - 1990-1999
    - 2000-Present
- Kodak Ventures Group
- Research & Development
- Careers@Kodak
- CEO Biography
- Chairman Biography
- Kodak Racing

1980 - Kodak celebrated its 100th anniversary. ♦ The company announced its entry into the clinical diagnostic market with the KODAK EKTACHEM 400 Analyzer, utilizing dry-chemistry blood serum analysis.

1981 - Company sales surpassed the $10 billion mark. ♦ Kodak acquired Atex, Inc., a manufacturer of computer-based publishing systems. ♦ The introduction of KODAK EKTAFLEX PCT Color Printmaking Products made it easy for home darkroom enthusiasts to make color enlargements.

1982 - Kodak launched "disc photography" with a line of compact, "decision-free" cameras built around a rotating disc of film. ♦ KODACOLOR VR 100 Film was introduced, utilizing a new T-GRAIN Emulsion Technology, which represented a major break-through in silver-halide emulsions. ♦ The Kodak pavilion opened in Walt Disney World's new EPCOT Center near Orlando, Florida.

1983 - Colby H. Chandler was elected chairman and chief executive officer and Kay R. Whitmore became president. ♦ The KODAK KAR 4000 Information System provided advanced capabilities for computer-assisted storage and retrieval of microfilm images. ♦ Tennessee Eastman began operation of the only commercial plant in the U.S. for making industrial chemicals from coal. ♦ The KODAK EKTACHEM DT60 Analyzer, a desk-top unit, brought the convenience of dry-chemistry blood serum analysis to the physician's office.

1984 - Kodak entered the video market with the KODAVISION Series 2000 8 mm video system and introduced KODAK Videotape Cassettes in 8 mm, Beta, and VHS formats. ♦ The company announced a full line of flexible floppy disks for personal computers.

1985 - The company introduced two new image management systems - the KODAK EKTAPRINT Electronic Publishing System (KEEPS) and the KODAK Information Management System (KIMS). ♦ Minilab systems for photofinishers were introduced, offering consumers exceptionally fast photo print service.

1986 - The company introduced two new KODACOLOR VR-G 35 Films and re-entered the 35 mm camera market with two new Kodak VR 35 Cameras. ♦ The company announced KODAK ULTRALIFE Lithium Power Cells, the world's first 9-volt lithium cells for consumer use, and entered the general consumer battery market with a line of KODAK

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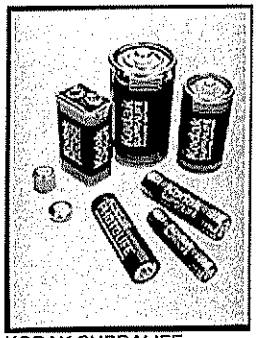
SUPRALIFE Batteries. ♦ Kodak entered a new health-care business with the establishment of its Eastman Pharmaceuticals Division.



KODAK SUPRALIFE Batteries.

1987 - The company entered the electronic still-video market with seven products for recording, storing, manipulating, transmitting and printing electronic still video images. ♦ Construction began on a new state-of-the-art sensitizing plant in Rochester, N.Y. for coating color films for professional use. ♦ Kodak announced its first one-time-use camera - the KODAK FLING Camera - which contained a 110 KODACOLOR Film Cartridge.

1988 - Kodak acquired Sterling Drug Inc., which provided the infrastructure and marketing ability Kodak needed to be a profitable participant in ethical and over-the-counter drugs. Kodak eventually sold its non-imaging health-related businesses in 1994. ♦ Qualex, Inc. was established as a joint venture between Kodak and Fuqua Industries, Inc., merging the operations of about 90 photographic processing labs owned by the two parties. ♦ The first line of color negative films created especially for photojournalists was introduced with Kodak EKTAPRESS GOLD films. ♦ Black-and-white film technology progressed with KODAK T-MAX P3200 film. ♦ The KODAK CREATE-A-PRINT 35 mm Enlargement Center enabled consumers to crop and make their own enlargements in a few minutes.

1989 - Kodak celebrated the 100th anniversary of motion pictures by introducing EASTMAN EXR Color Negative Films. ♦ The KODAK XL 7700 Digital Continuous Tone Printer, which produced large format thermal color prints, was introduced. ♦ The one-time-use KODAK STRETCH 35 Camera produced 3 1/2 x 10 - inch prints for panoramic scenes. ♦ The one-time-use KODAK WEEKEND 35 Camera was an all-weather camera capable of taking pictures underwater down to a depth of 8 feet. ♦ The KODAK IMAGELINK Component Series (for document imaging) and KODAK OPTISTAR Products (for computer output) offered a choice of micrographic or digital capture of images. ♦ The KODAK X-OMATIC RA cassette significantly reduced radiographic exposure for pediatric patients. One-time-use KODAK FUN SAVER Panoramic 35 Camera

One-time-use KODAK FUN SAVER Panoramic 35 Camera.

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EXHIBIT 42

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EXHIBIT 43

US005440343A

United States Patent [19]

Parulski et al.

[11] Patent Number: 5,440,343

[45] Date of Patent: Aug. 8, 1995

[54] MOTION/STILL ELECTRONIC IMAGE SENSING APPARATUS

[75] Inventors: Kenneth A. Parulski; Eric G. Stevens, both of Rochester; Robert H. Hibbard, Fairport, all of N.Y.

[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 203,237

[22] Filed: Feb. 28, 1994

[51] Int. Cl.[6] H04N 5/335

[52] U.S. Cl. 348/316; 348/322; 348/220

[58] Field of Search 348/207, 220, 294, 316, 348/317, 311, 314, 315, 322, 323, 297; H04N 5/335

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5-37861	2/1993	Japan	H04N 5/335

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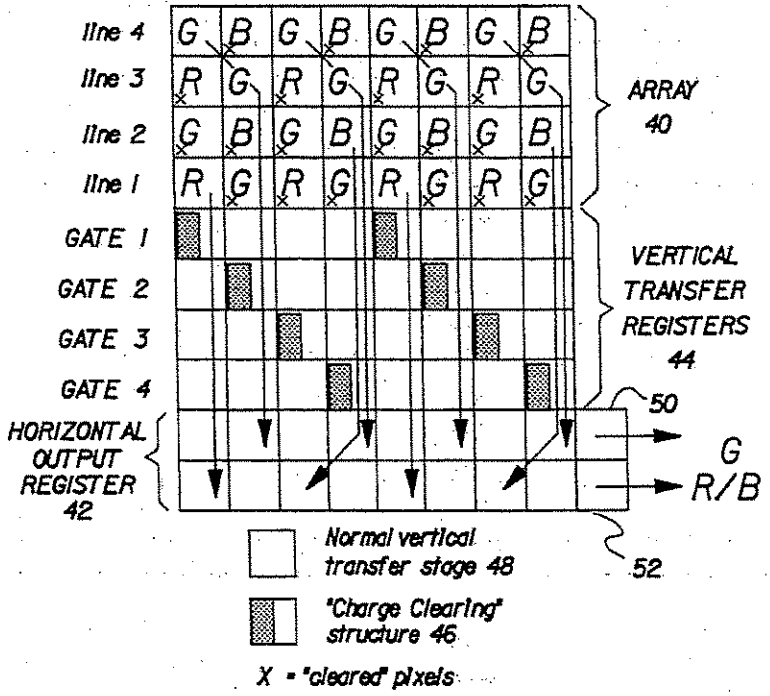
KAI-1001 Series—1024(H)×1024(V) Pixel-Megapixel Interline CCD Image Sensor Performance Specification—Eastman Kodak Company—Apr. 26, 1993.

Primary Examiner—Michael T. Razavi
Assistant Examiner—Tuan V. Ho
Attorney, Agent, or Firm—David M. Woods

[57] ABSTRACT

An electronic imaging system is provided that records both motion and still video images. In a motion mode of operation, the electronic imaging system records NTSC resolution images at a standard thirty frame per second rate. In a still mode of operation, the electronic imaging system records megapixel resolution still images at a much lower frame rate. The electronic imaging system utilizes an electronic image sensor that incorporates column selective "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain color pixels. The charge parking structures are used to sum the charge from multiple vertical pixels. The architecture of the electronic image sensor also allows different image aspect ratios to be provided for the motion and still modes described above.

12 Claims, 10 Drawing Sheets



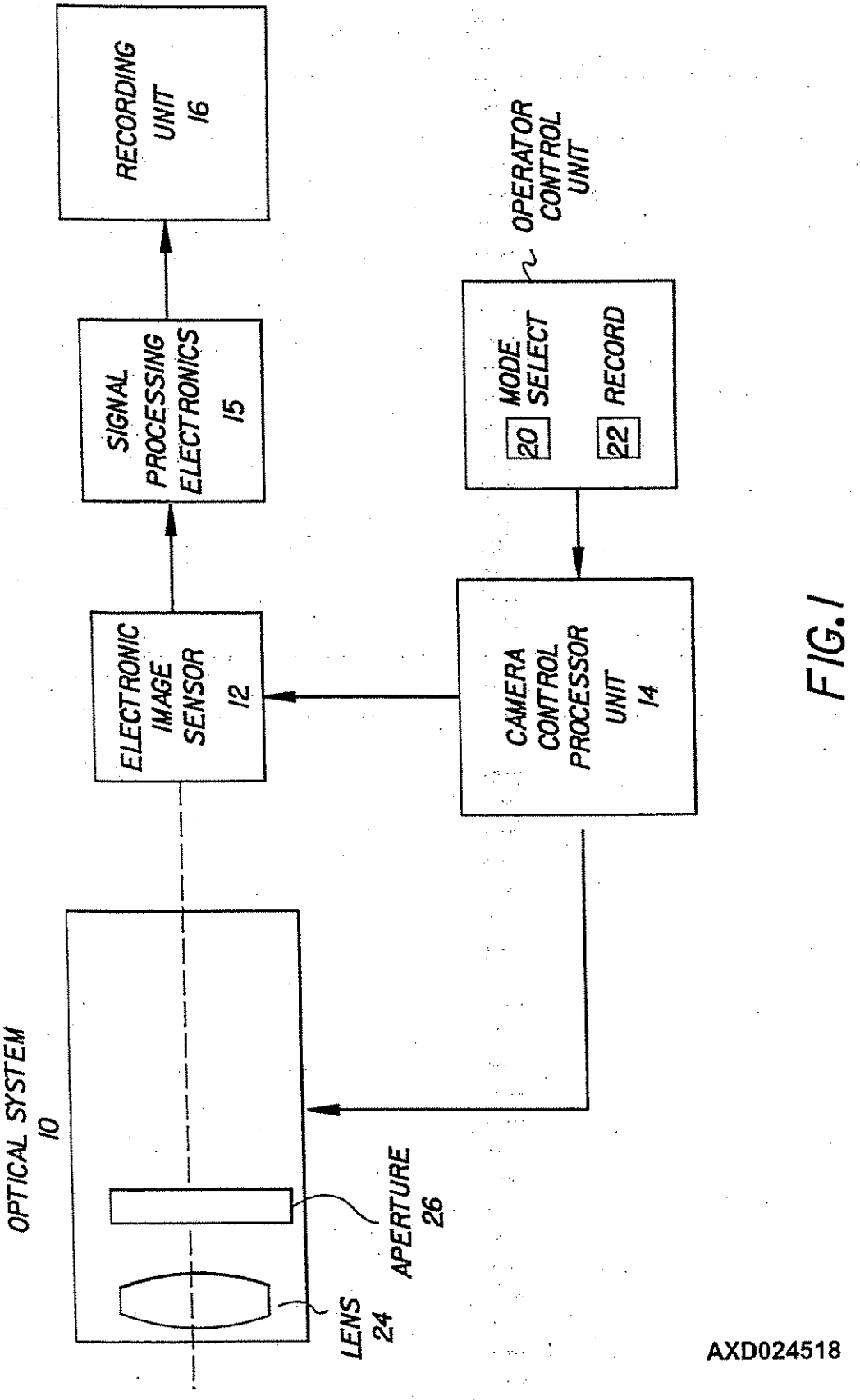


FIG. 1

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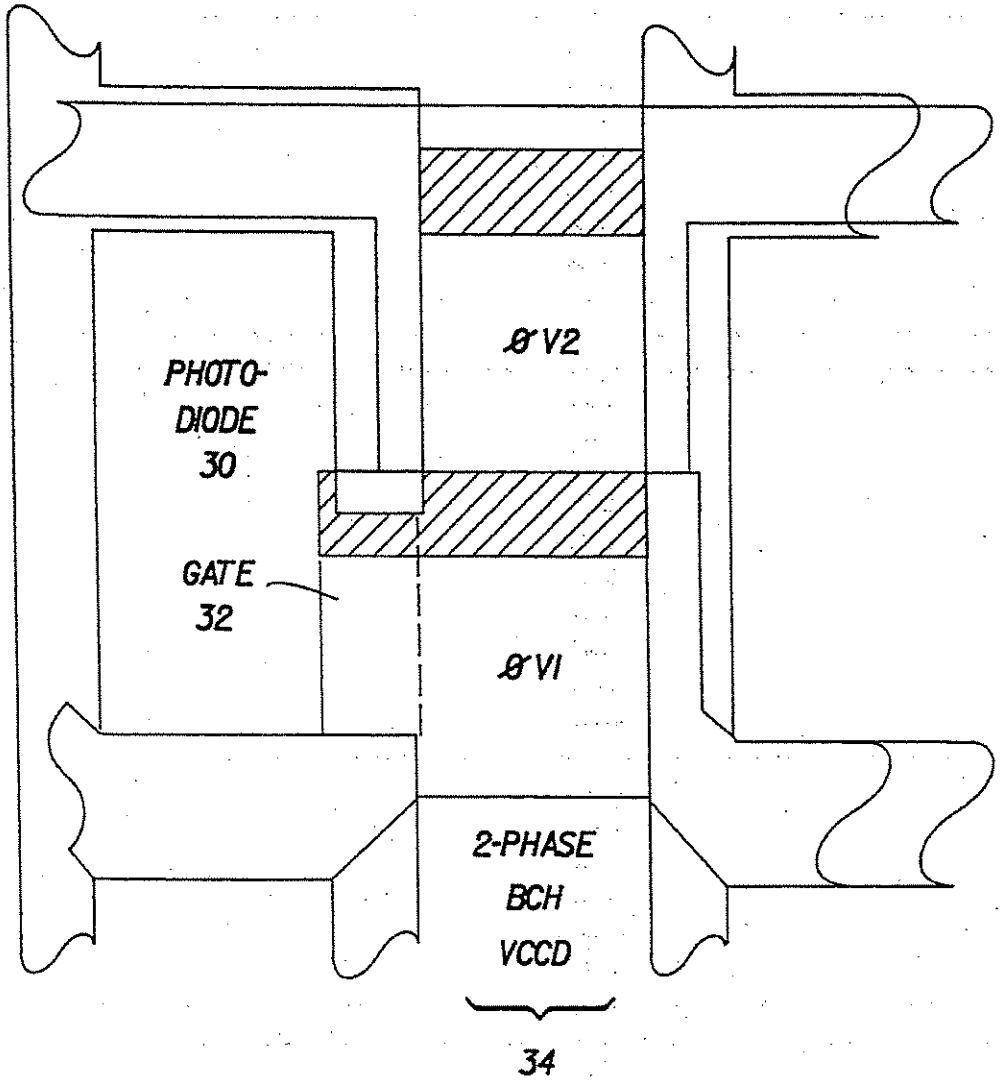

FIG. 2

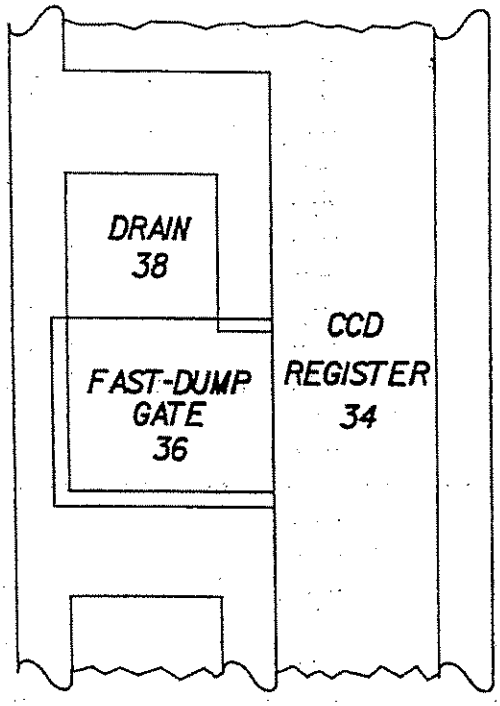
DRAIN
38
FAST-DUMP
GATE
36
CCD
REGISTER
34

FIG. 3

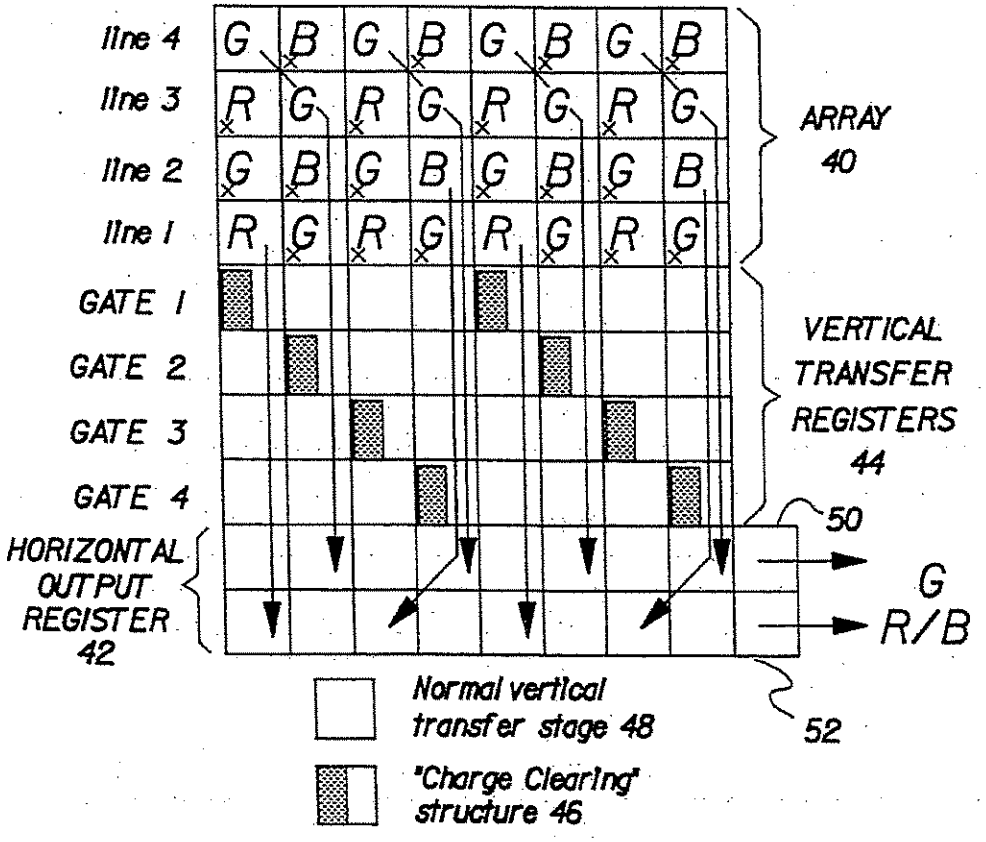
line 4
line 3
line 2
line 1
GATE 1
GATE 2
GATE 3
GATE 4
HORIZONTAL
OUTPUT
REGISTER
42
ARRAY
40
VERTICAL
TRANSFER
REGISTERS
44
50
G
R/B
52
Normal vertical
transfer stage 48
"Charge Clearing"
structure 46
X = "cleared" pixels
AXD024520

FIG. 4

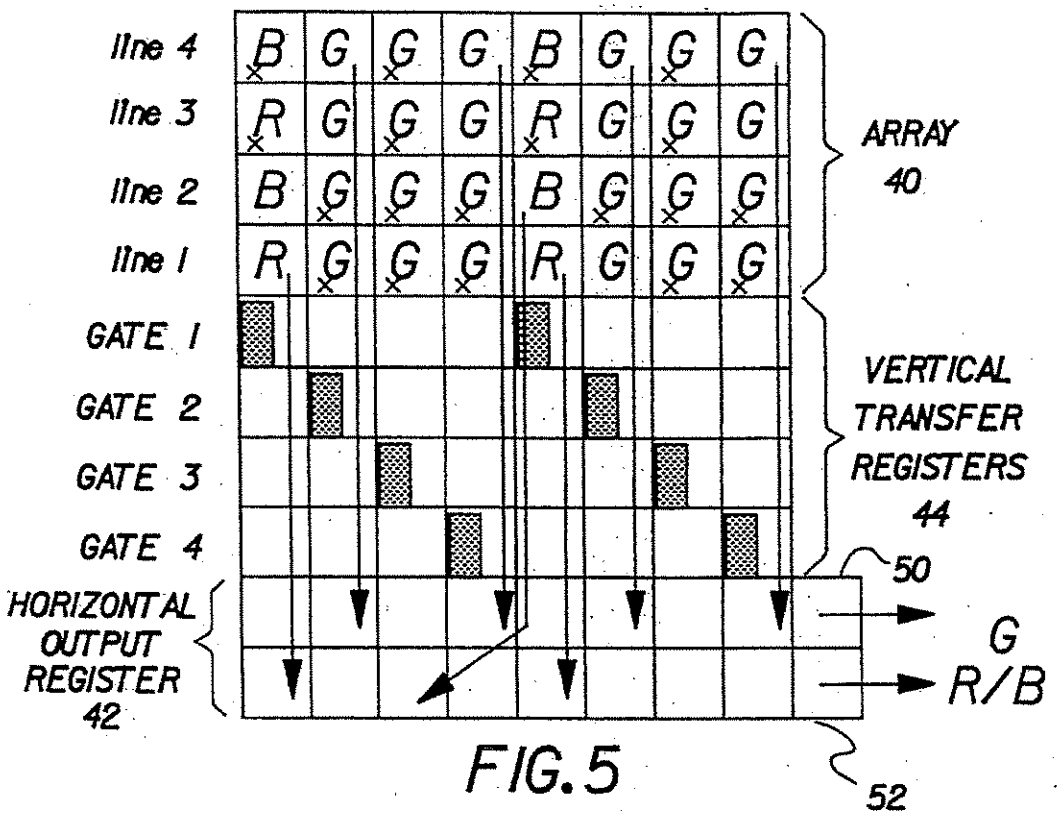

FIG. 5

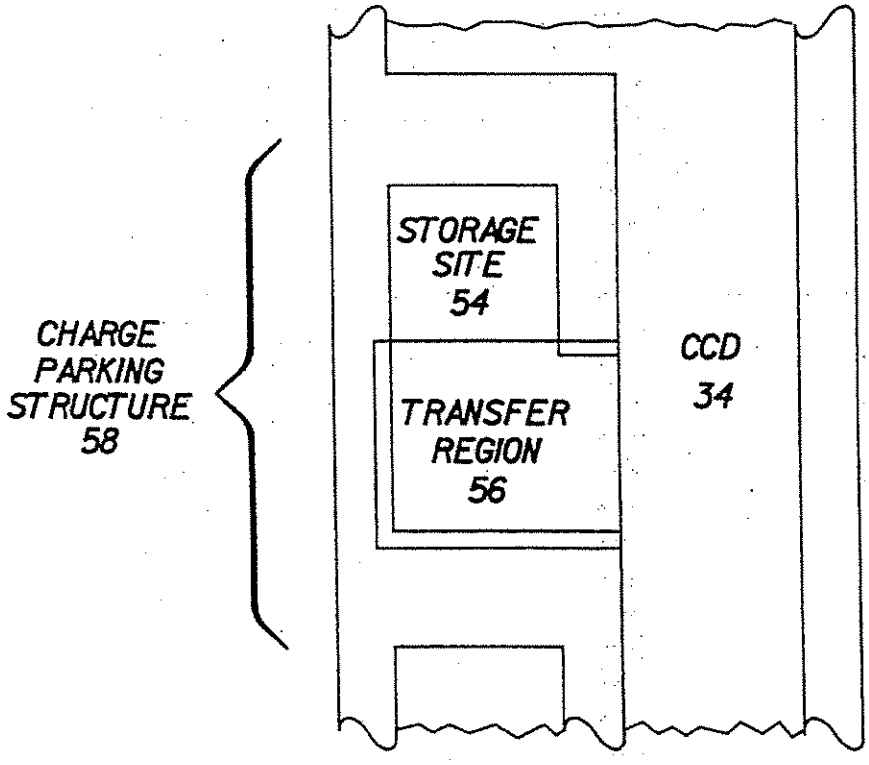

FIG. 6

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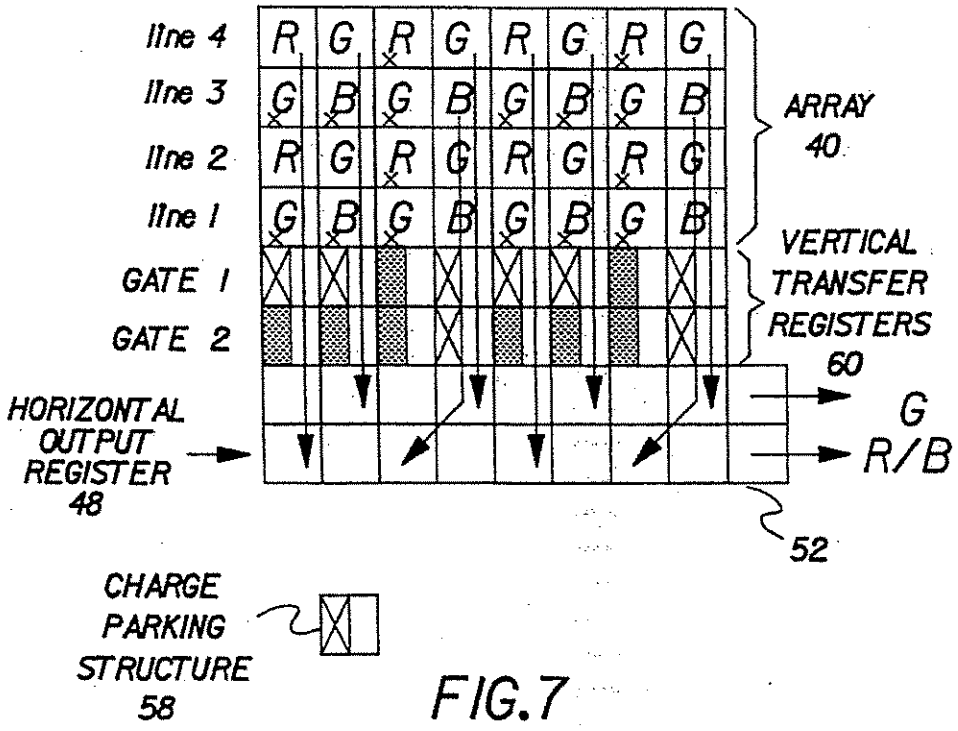

FIG.7

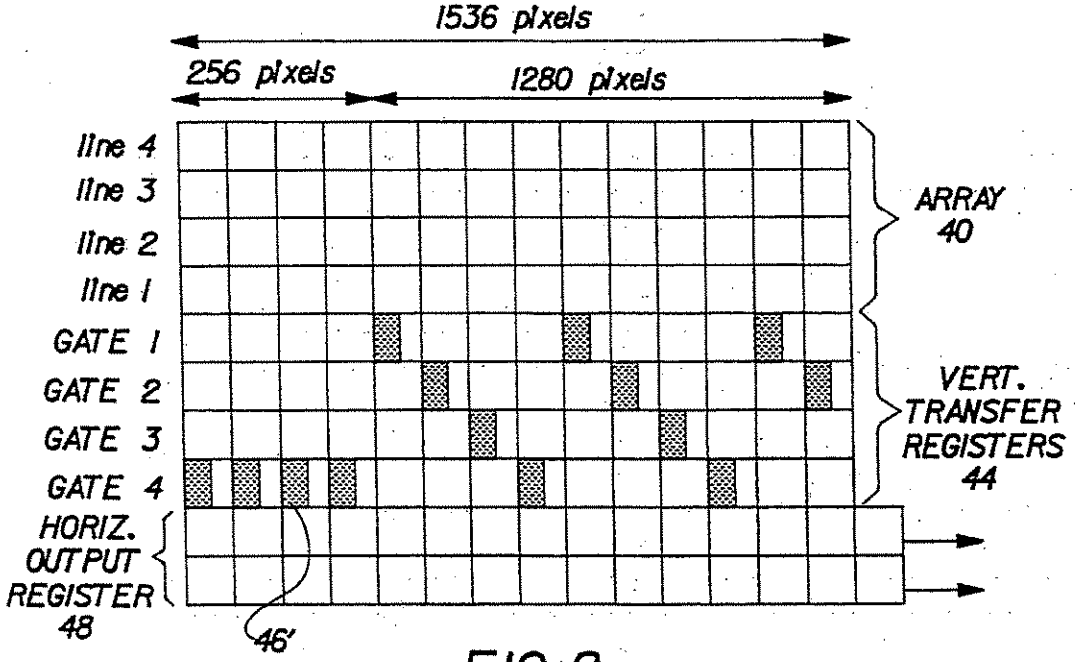

FIG.8

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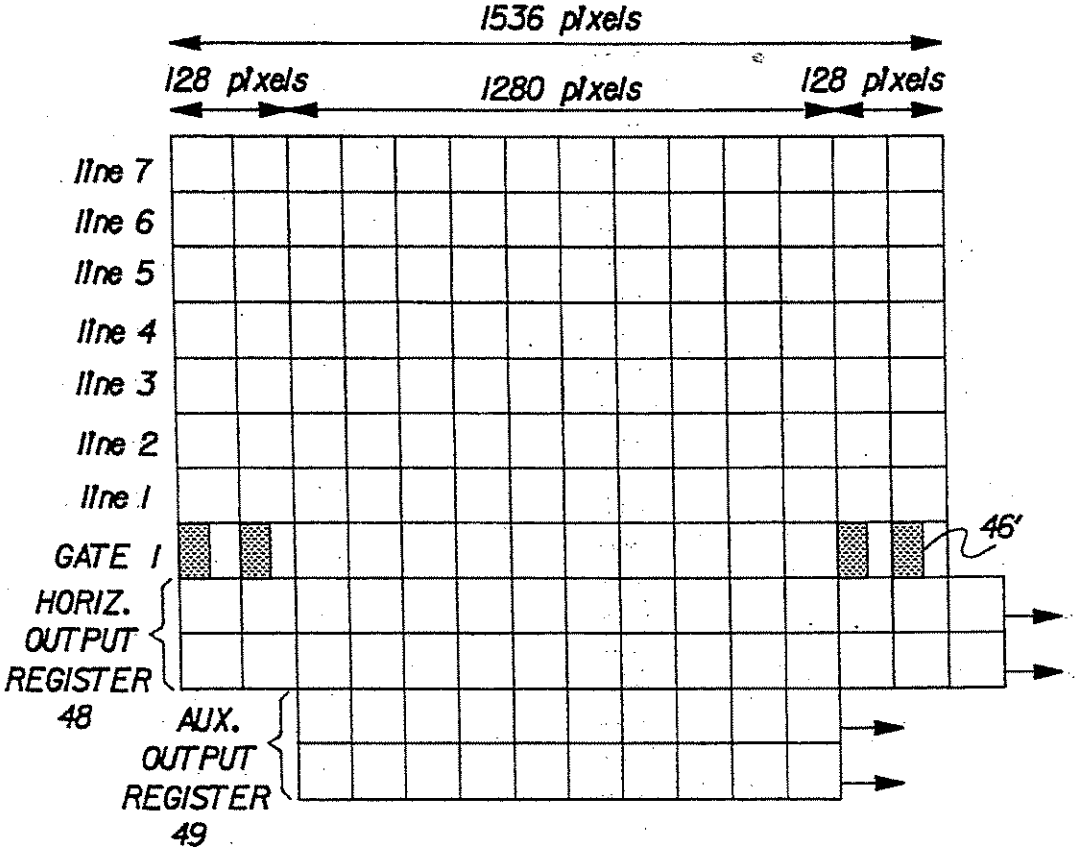
1536 pixels
128 pixels
1280 pixels
128 pixels
line 7
line 6
line 5
line 4
line 3
line 2
line 1
GATE 1
46'
HORIZ. OUTPUT REGISTER 48
AUX. OUTPUT REGISTER 49

FIG. 9

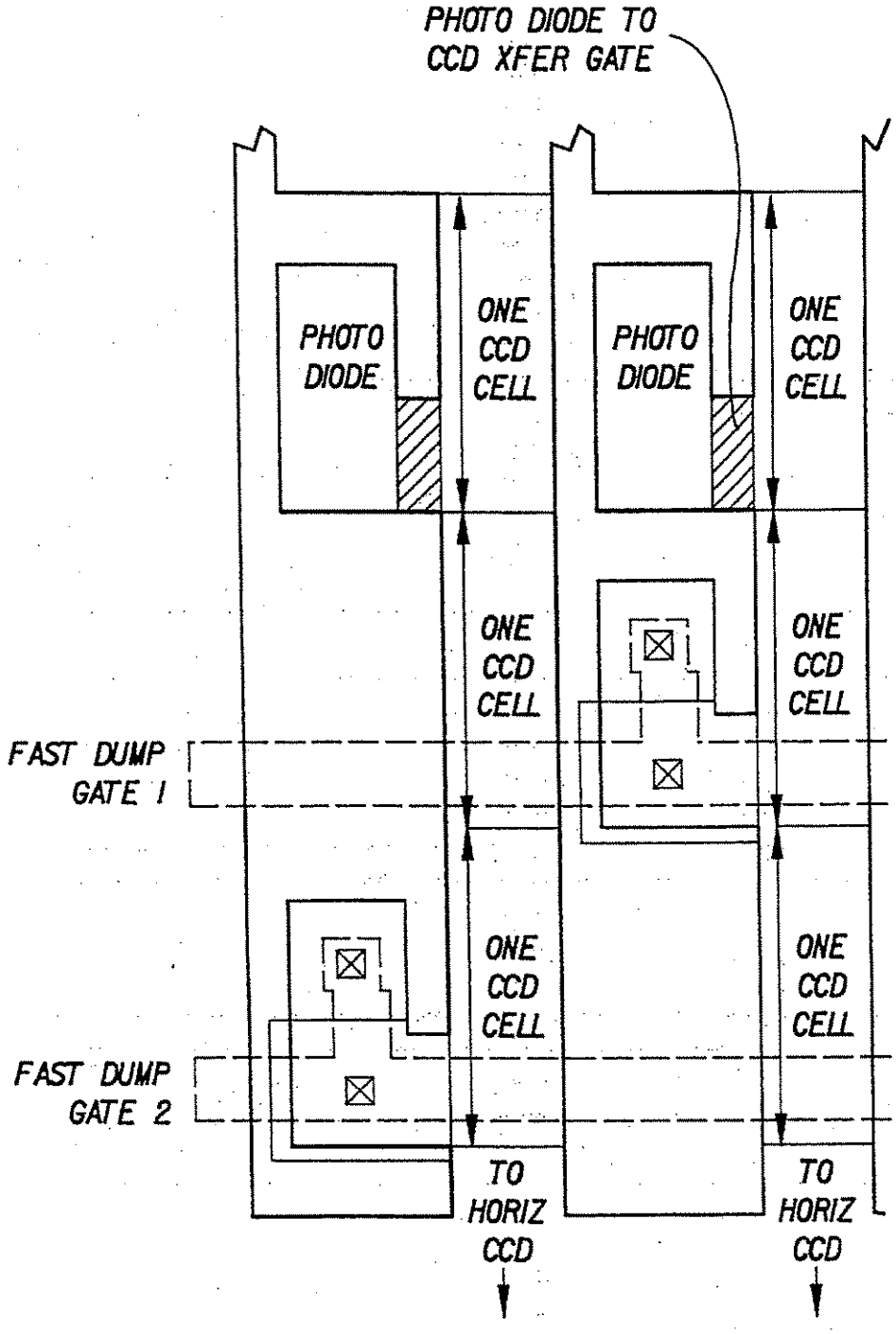

FIG. 10

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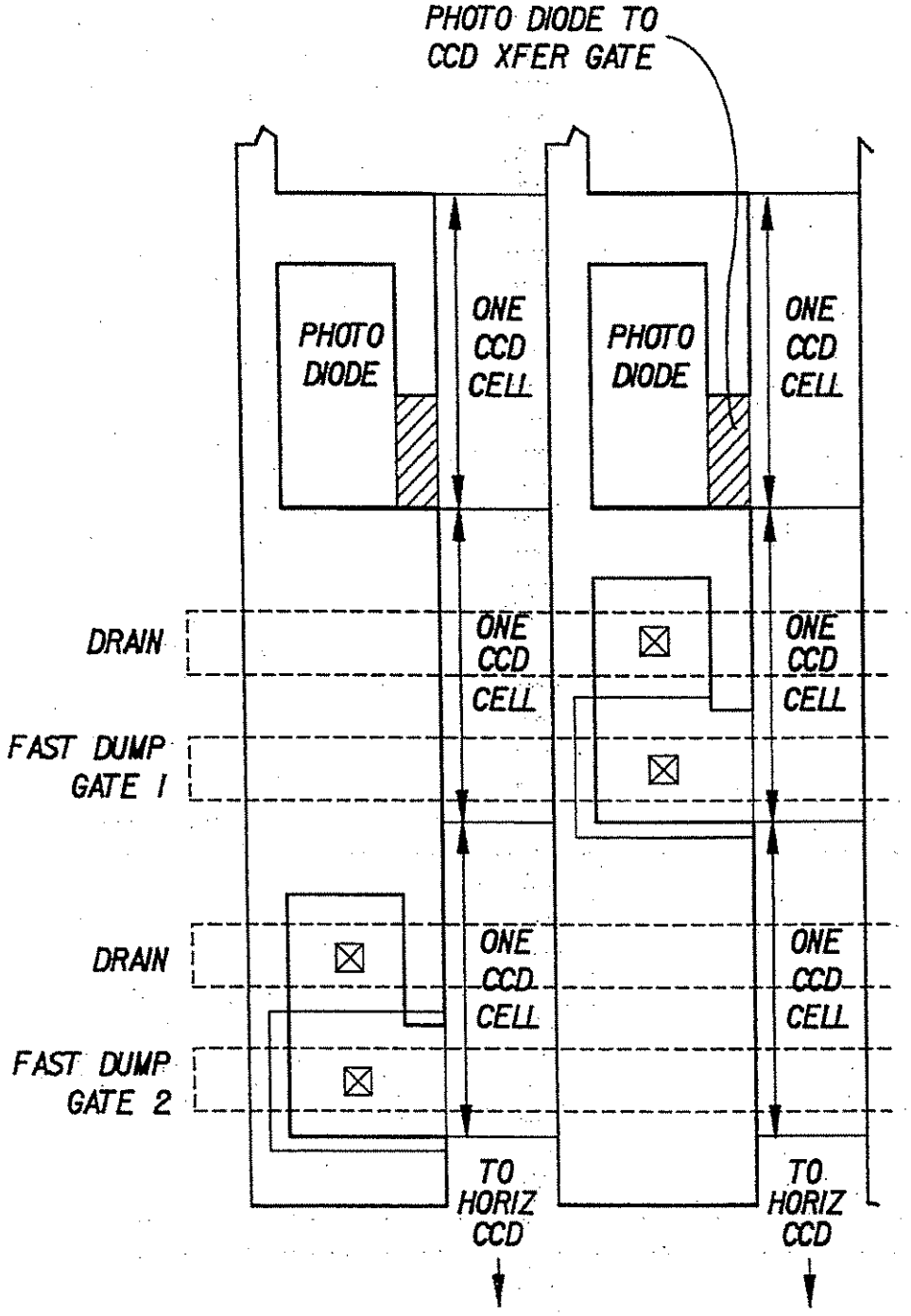

FIG. 11

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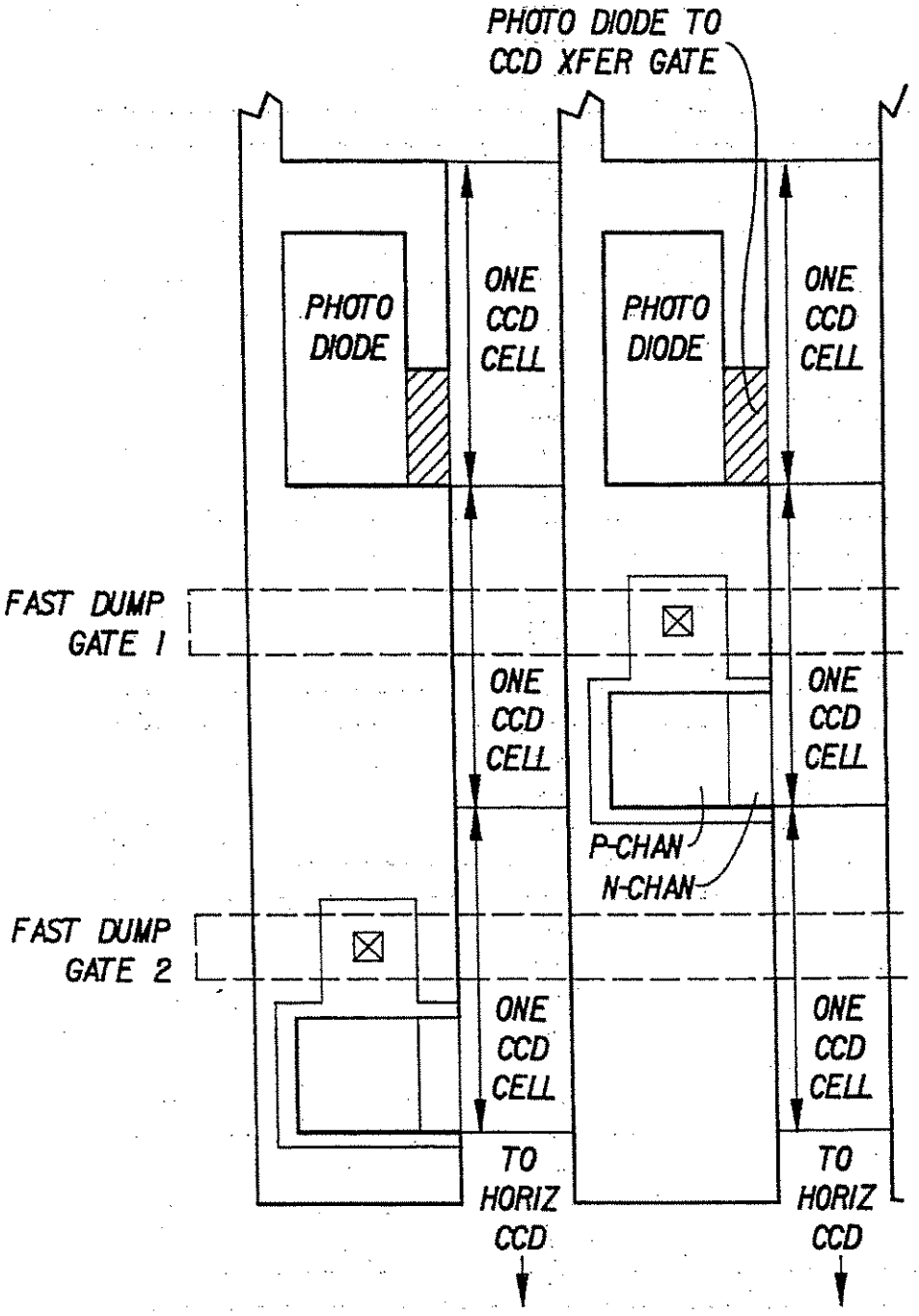

FIG. 12

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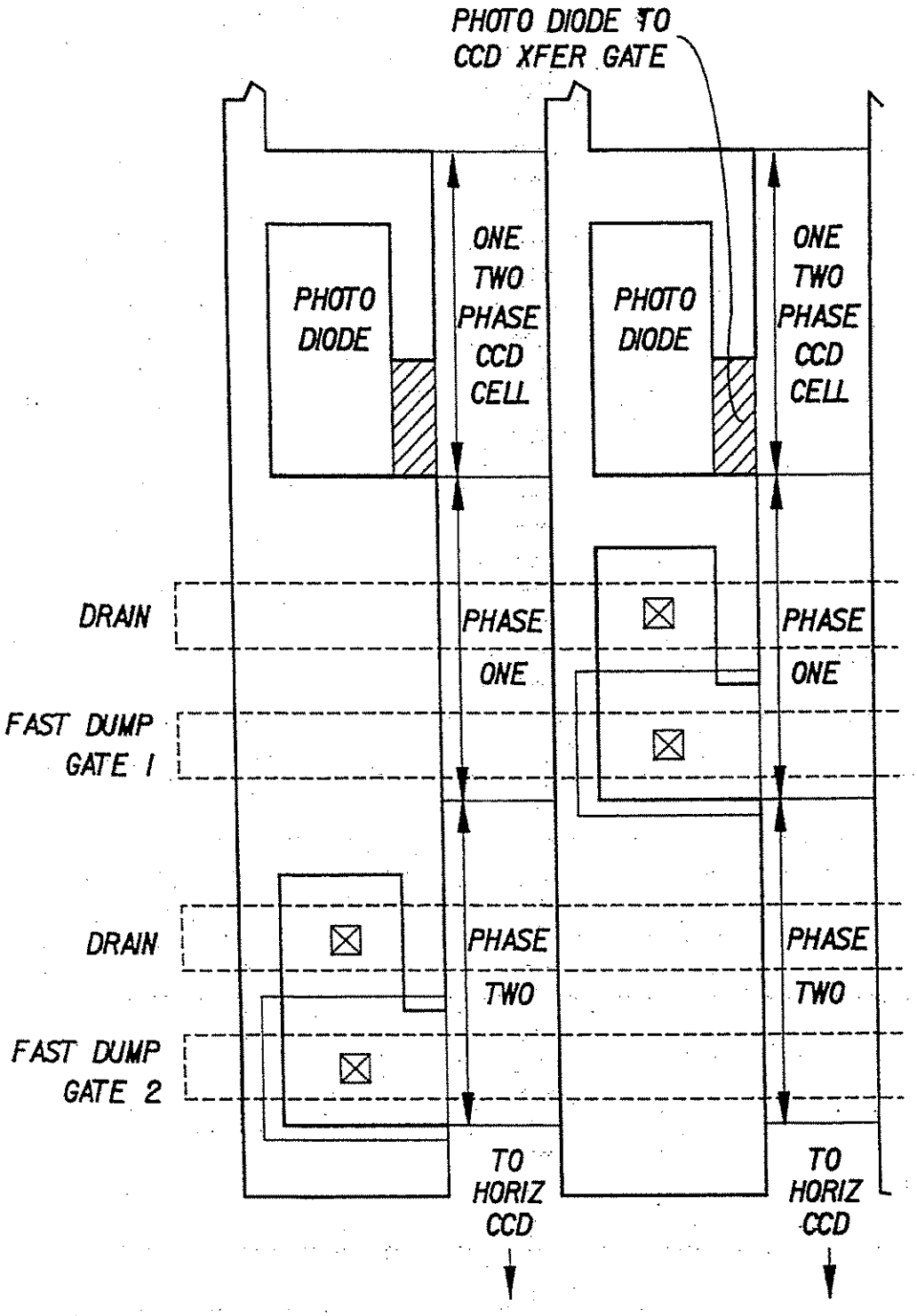

FIG. 13

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MOTION/STILL ELECTRONIC IMAGE SENSING APPARATUS

FIELD OF THE INVENTION

The invention relates generally to an electronic imaging system. More specifically, the invention relates to an electronic imaging system for capturing images in both a motion mode and a still mode, wherein the electronic imaging system captures medium resolution motion images at a standard frame rate and high resolution still images at a much lower frame rate.

BACKGROUND OF THE INVENTION

Motion/still electronic imaging systems including the capability of recording analog motion images and digital still images on the same recording medium, for example 8 mm or VHS format magnetic tape, have recently been developed by a number of manufacturers. The motion/still camcorders currently available record motion images in the same manner as conventional motion only video recording cameras. In order to record still images, the user activates an operator control to switch to a "still" mode of operation in which image data generated from the systems electronic image sensor is temporarily stored in a digital memory for subsequent recording onto videotape.

Conventional motion/still camcorders utilize the same type of NTSC resolution interlaced electronic image sensors originally developed for motion only electronic camera systems. Although the conventional image sensors provide sufficient data to produce relatively low resolution analog NTSC signals, the image sensors are not capable of generating still images having the high resolution associated with high quality electronic still imaging systems. Some current electronic still imaging systems, for example, are capable of recording over one thousand lines of image information, while only 480 lines of image information are required for one frame of an NTSC video signal.

Of course, a high definition television (HDTV) electronic image sensor could be used in a motion/still camcorder to directly obtain high resolution still images and HDTV motion images, but downconversion would be required to obtain NTSC motion images. In such a case, the electronic image sensor must be capable of operating at pixel data rates of greater than 50M pixels/second. Electronic image sensors capable of operating at such high pixel data rates, however, are typically very costly to produce and have much higher power consumption rates than conventional NTSC compatible sensors.

In view of the above, it is an object of the invention to provide an electronic imaging system that is capable of producing NTSC motion images and high resolution still images. It is a further object of the invention to provide an electronic image sensor for the electronic imaging system, which can be operated in a low resolution mode to provide NTSC resolution motion scenes at the standard thirty frames/second rate, and operated in a high resolution mode to provide high resolution still images at slower frame rates. It is a still further object of the invention to provide an electronic image sensor, as described above, that is less expensive to produce and has lower power consumption requirements than HDTV electronic image sensors.

SUMMARY OF THE INVENTION

The invention provides an electronic imaging system that records both motion and still video images. In a motion mode of operation, the electronic imaging system records NTSC resolution images at a standard thirty frame per second rate. In a still mode of operation, the electronic imaging system records megapixel resolution still images at a much lower frame rate.

The electronic imaging system utilizes an electronic image sensor that includes an array of photosensitive picture element sites, or "pixels" which collect photogenerated charge packets. Each charge packet is a pixel image signal. Image signals are generated from all of the pixels in the still mode of operation. In the motion mode of operation, however, the image signals generated from certain selected pixels are discarded or combined with the signals from nearby pixels in order to generate images at thirty frames per second while using a standard video rate output pixel clock (approximately 12 MHz) instead of an HDTV rate pixel clock (>50 MHz). The electronic image sensor incorporates column selective fast dump "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain color pixels. The charge parking structures are used to sum the charge from non-adjacent vertical pixels. The architecture of the electronic image sensor also allows different image aspect ratios to be provided for the motion and still modes described above.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in greater detail with reference to the accompanying drawings wherein:

FIG. **1** is a block diagram of an electronic imaging system in accordance with the invention;

FIG. **2** illustrates an image pixel site of the type incorporated in the electronic image sensor shown in FIG. **1**;

FIG. **3** illustrates a charge clearing structure of the type incorporated in the electronic image sensor shown in FIG. **1**;

FIG. **4** illustrates a first embodiment of the electronic image sensor shown in FIG. **1**;

FIG. **5** illustrates the use of a different color filter array with the electronic image sensor structure shown in FIG. **4**;

FIG. **6** illustrates a charge parking structure utilized in a second embodiment of the invention;

FIG. **7** illustrates an electronic image sensor in accordance with a second embodiment of the invention that utilizes the charge parking structure illustrated in FIG. **6** and the charge clearing structure illustrated in FIG. **3**;

FIG. **8** illustrates a third embodiment of the invention that incorporates aspect ratio conversion;

FIG. **9** illustrates a fourth embodiment of the invention that incorporates aspect ratio conversion;

FIGS. **10–12** illustrate three methods of creating column selectable "charge clearing" structures using 2 CCD phases per row; and

FIG. **13** illustrates a "charge clearing structure using 1 CCD phase per row.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A motion/still electronic imaging system according to the invention is illustrated in FIG. **1**. The imaging system includes an optical system **10**, a motion/still

electronic image sensor **12**, a camera control processor unit **14**, signal processing electronics **15**, a recording unit **16**, and an operator control unit **18**, which includes a mode selection switch **20** and a record or "shutter" control switch **22**. An optional flash unit may also be incorporated in the structure of the imaging system or as an accessory item. The optical system **10** of the illustrated embodiment includes a lens **24**, and an adjustable aperture **26**, which are controlled by the camera control processor unit **14**. It will be understood that the invention is not limited to the use of illustrated optical system **10**, but is also applicable to imaging systems using any type of known optical system, including those using fixed apertures and systems that utilize mechanical shutter devices.

In operation, a user places the mode switch **20** in a "motion" mode position and depresses the record switch **22** to record motion images. The camera control processor unit **14** controls the operation of the electronic image sensor **12**, the signal processing electronics **15**, and the recording unit **16** in order to record the output of the electronic image sensor. The recording unit **16** preferably includes a digital magnetic tape recording unit, so that the processed sensor output signal is recorded on a magnetic tape located in the recording unit **16** as an NTSC resolution video image sequence until the record switch **22** is released. To record a still image, the user places the mode switch **20** into the "still" mode position, so that a high resolution still image is captured and recorded by the recording unit **16** each time the record switch **16** is depressed. The recording unit **16** preferably includes digital memory means for storing the still images (for example Flash EPROM memory cards) in addition to the magnetic tape recording unit, although the still images can also be stored on tape if desired.

The electronic image sensor **12** includes a row and column array of pixels that generate signal in response to the amount of radiation incident thereon and at least one horizontal output register. A conventional color filter array (not shown) is provided so that selected pixel sites generate image signals corresponding to red, green and blue color components. In addition to the photosensitive pixels, the electronic image sensor includes column selective "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain pixels, while the charge parking structures are used to add the charge from non-adjacent vertical pixels.

FIG. **2** illustrates a top view of one photosensitive pixel of the type included in the array of the electronic image sensor **12**. The pixel is of conventional construction, and is preferably of the type incorporated in the KAI-1001 interline image sensor manufactured by the Eastman Kodak Company of Rochester, N.Y. The design and operation of this image sensor is described in "KAI-1001 series Megapixel Interline CCD Image Sensor Performance Specification, " Rev. 1 April 1993, available, from the Microelectronics Technology Division of Eastman Kodak Company, and in "A 1 Megapixel, Progressive-Scan Image Sensor with Anti-blooming Control and Lag-Free Operation" by E. G. Stevens, et al., IEEE Trans. Electron Devices, Vol. 38, May 1991, both of which are incorporated by reference herein. The 9×9 micron pixel site includes a photodiode **30**, a transfer gate **32** and a two-phase CCD register **34**. The operation of the photosite is well known in the art and need not be discussed in great detail.

FIG. **3** illustrates a top view of one of the charge clearing structures incorporated in the electronic image sensor **12**. The charge clearing structures are located in selected columns of at least one row of vertical transfer registers located between the two-dimensional array of photosites and a horizontal output register of the electronic image sensor **12** as will be described in greater detail below. The charge clearing structure includes a fast dump gate **36** and a drain **38** located adjacent to the CCD register **34**. The fast dump gate **36**, when activated, permits charge being transferred in the CCD register **34** to be dumped to the drain **38**. The drain **38** may be a separate electrode, as shown in FIG. **11**, or, as shown in FIG. **10**, it may contact a polysilicon and a metal drain line connected via a bond wire to an external control pin on the sensor package, which is held at an appropriate potential so as to drain the charge from CCD register **34**.

FIGS. **10–12** show different charge clearing structures using one true two-phase CCD cell per row. It is also possible to use charge clearing structures having only one of the two CCD cells per row. This reduces the number of vertical transfer required to transfer the first line of charge from the photosensitive pixel array to the horizontal readout register. FIG. **10** illustrates the use of a surface-channel, fast-dump gate ($V_T>0$) so that the drain may be connected to the gate, thereby saving a pin. FIG. **11** shows a structure providing a separate gate and drain electrode, as would be required for a buried-channel, fast-dump gate ($V_T>0$). FIG. **12** shows a charge-clearing structure of a vertical type wherein the drain **38** lies below the gate (the n-type substrate). FIG. **13** shows a charge-clearing structure similar to that of FIG. **11**, except that the gate **1** row charge clearing structure is adjacent to phase one of a two phase CCD cell, and the gate **2** row charge clearing structure is adjacent to phase two of the same CCD cells whereas in FIG. **11**, each charge clearing structure is adjacent to a two phase CCD cell.

A preferred image sensor architecture incorporating photosensitive pixels of the type illustrated in FIG. **2** and charge clearing structures of the type illustrated in FIG. **3** is shown in FIG. **4**. For purposes of simplification, an array **40** of image pixel sites is shown having just four image lines, although it will be understood that any number of image lines of any desirable length may be employed. The four image lines are separated from a horizontal output register **42** by four rows of vertical transfer registers **44**, wherein each row of vertical transfer registers **44** includes at least one charge clearing structure **46** and a plurality of normal or conventional vertical transfer stages **48**. The charge clearing structures **46** in each row of vertical transfer registers **44** are respectively controlled by "gate 1", "gate 2", "gate 3" and "gate 4" signals supplied by the camera control processor unit **14** illustrated in FIG. **1**. The image pixel sites are arranged in accordance with a Bayer color filter array pattern as described in U.S. Pat. 3,971,065, "Color Imaging Array" by B. E. Bayer, assigned to Eastman Kodak Co. and incorporated herein by reference, with green photosites arranged in a checkerboard pattern and red and blue pixels arranged on alternate lines. The horizontal output register **42** includes a first horizontal transfer register **50** for green image pixel signals and a second horizontal transfer register **52** for red and blue image pixel signals.

In operation, signal charge packets from each of the lines of photoactive pixels are clocked through the four rows of vertical transfer registers **44** including the charge clearing structures **46**. When a given line is clocked from the imaging array into the "gate **1**" row of vertical transfer registers **44**, for example, the signal charge from the first and fifth columns of the line is transferred to the drains **38** of the charge clearing structures **46** if the gate **1** signal is activated. In all other columns of the line (for example columns **2, 3, 4, 6, 7**) the signal charge is unaffected. If the gate **1** signal is turned off, the charge clearing structures **46** in the gate **1** row of vertical transfer registers **44** are disabled, and the signal charge packets transferred from the array **40** to the gate **1** row are unaffected. By incorporating four "charge clearing" rows having charge clearing structures **46** offset in different columns, it is possible to eliminate all of the signal charge packets from a given image line by turning on the "clear" signals as the line of image pixel signals passes through the gate **1**, gate **2**, gate **3** and gate **4** vertical transfer rows **44**.

In a still mode of operation, all of the charge clearing structures **46** are disabled, thereby allowing all of the signal charge packets to be clocked into the horizontal output register **42**. The green image pixel signals are subsequently clocked out of the first horizontal transfer register **50** and the red and blue image pixel signals are clocked out of the second horizontal transfer register **52**. The color filter array pattern is designed to provide the best image possible in the high resolution still mode of operation.

An NTSC resolution image is obtained in a motion mode of operation by selectively activating the charge clearing structures **46**. As line one of the image passes through the vertical transfer registers **44**, gate **1** is turned off, but gate **2**, gate **3** and gate **4** are turned on. Thus, only the red image pixel signals associated with every other odd column, i.e. columns **1, 5, 9**, etc., are transferred to the horizontal output register **42**. The image pixel signals representing the green pixels and the alternate red pixels of line one are drained off by the activated charge clearing structures **46**. In order to read out image line **2**, the gate **4** signal is turned off and the other three signals are turned on, thus passing every other blue image pixel signal to the horizontal output register **42**. Following the transfer of the blue image pixel signals, the second horizontal transfer register is clocked once to put the blue pixels in their proper location. All of the green image pixel signals for the third image line are kept by deactivating all of the charge clearing structures **46** as the third image line is clocked through the rows of vertical transfer registers **44**. The fourth line of image pixel signals can either be eliminated by turning on all four gate signals or can also be passed to the first horizontal transfer register **50** and summed with the green pixels from the other image lines. The next field of the NTSC signal is "staggered" vertically by shifting the sampling by two lines in the vertical direction.

FIG. **5** shows how the same basic image sensor architecture illustrated in FIG. **4** can be used with a different color filter array pattern, for example a "3G" non-interlaced striped CFA, as described in U.S. Pat. No. 4,663,661 "Single Sensor Color Video Camera with blurring filter" by J. S. Weldy and S. H. Kristy, assigned to Eastman Kodak Company and incorporated herein by reference, to generate an NTSC signal. In this example, the red and blue image pixel signals are clocked into the horizontal output register **42** by turning off the gate **1** signal and turning on the gate **2**, gate **3** and gate **4** signals. The second horizontal transfer register **52** is clocked twice before summing. The third and fourth image lines are clocked into and summed in the horizontal output register by turning off the gate **2** and gate **4** signals and turning on the gate **1** and gate **3** signals. The fourth image lines can alternatively be discarded by turning on the gate **2** and gate **4** signals. As in the case illustrated in FIG. **4**, a still mode of operation is obtained by deactivating all of the gate signals.

Referring now to FIG. **6**, a charge "parking" or storage structure **58** is shown including a storage site **54** and a transfer gate or region **56** located adjacent to the CCD register **34**. The charge parking structure **58** is used in conjunction with the charge clearing structure **46** described above in a second embodiment of the invention. In operation, the transfer region **56** of the charge parking structure **58** is activated to transfer a signal charge packet from the CCD register **34** to the storage site **54**. The storage site **54** can be used to sum signals from different non-adjacent rows of the array of pixels.

The charge is stored by setting the channel potential of the storage site **54** to a higher potential than the transfer region **56**, which is likewise at a higher channel potential than the adjacent CCD register **34**. To later sum the stored charge with a non-adjacent row of charge which has been shifted into CCD register **34**, the channel potential of the CCD register **34** must be brought higher than that of the transfer region **56**, which must be higher than that of the storage site **54**. Otherwise, during readout of CCD register **34**, the transfer region **56** is brought to a lower channel potential than in CCD register **34** or the storage site **54** to create a barrier and prevent the transfer of charge between them.

FIG. **7** illustrates an electronic image sensor in accordance with a second embodiment of the invention. The image sensor is shown having four image lines and two rows of vertical transfer registers **60** which include both charge clearing structures **46** and charge parking structures **58**. As in the structure illustrated in FIG. **5**, electronic image sensor also includes a horizontal output register **42** having first and second horizontal transfer registers **50, 52** as shown in FIGS. **4** and **5**.

In operation, the charge clearing structure **58** location in column four of the gate **2** row, for example, allows the blue pixel values from image line one and image line three to be summed, even though there is a green pixel value between these two blue values. To obtain an NTSC resolution image, image lines **1** and **2** are clocked into the gate **1** and gate **2** rows. In the gate **2** row, the image line **1** blue pixel values from columns **4, 8**, etc. are parked or stored while the green pixels and the remaining blue pixels are cleared discarded. In the gate **1** row, the green pixels and alternate red pixels are parked while the remaining red pixels are discarded or cleared. Image lines three and four are subsequently clocked into the gate **1** and gate **2** rows. In the gate **2** row, the line **3** blue pixel values from columns **4, 8** etc. are summed with the line one blue pixel values, while the green pixels and the remaining blue pixels are cleared. In the gate **1** row, the line **4** red pixel values from columns three and seven etc are cleared, while the green pixels and the remaining red pixels are summed with the values in the charge parking registers. Finally, the image pixel signals are transferred into the horizontal output register.

One additional problem with NTSC motion/still systems is that it may be desirable to use different image aspect ratios for the motion and still modes. For example, NTSC uses a 4:3 aspect ratio image, while the requirement for high resolution stills may be a 3:2 aspect ratio as utilized, for example, in the Kodak Photo CD System. The electronic image sensor is therefore required to have a 1024×1536 image array to provide a 3:2 aspect ration, while for the NTSC mode, it might be desirable to use only 960×1280 pixels from the electronic image sensor to provide a 4:3 aspect ratio image.

A method of facilitating the readout of different aspect ratio images is shown in FIG. 8. The structure shown in FIG. 8 utilizes 256 "aspect ratio charge clearing" structures 46' of the type shown in FIG. 3 placed in the end of at least one row of the vertical transfer registers 44, between the image array 40 containing the photosensitive pixels, and the horizontal output register 48. When activated by a signal supplied by the camera control processor unit 14, the aspect ratio charge clearing structures 46' eliminate the signals from the columns at the left side of the image array 40 as the image lines are clocked out. As a result, the horizontal output register 48 does not receive charge from these columns.

It should be noted that there is insufficient time to clock out all of the 256 extra pixels at the end of each NTSC image line, so that charge from these extra pixels would end up at the right hand side of the horizontal readout register 48 without the use of the aspect ratio charge clearing structures 46'. In such a case, this charge would be added to the right side of the next new line of the image causing a serious artifact. The aspect ratio charge clearing structures 46' eliminate the signals from these pixels so that the next image line contains only the proper signal charge, namely, only the 1280 horizontal pixels needed to be clocked out.

A second embodiment that compensates for the differences in aspect ratios is shown in FIG. 9. The second structure utilizes a second auxiliary horizontal output register 49. The second horizontal output register 49 is centered in the middle of the image array 40 and has 256 fewer elements than the normal horizontal output register 48. Aspect ratio charge clearing structures 46' are used to dispose of the charge in the first and last 128 columns of the image array which are not used in the NTSC readout mode.

The invention has been described with reference to certain preferred embodiments thereof. It will be understood, however, that modifications and variations are possible within the scope of the appended claims. For example, the aspect ratio charge clearing structures need not be located within the same row of vertical transfer registers, but can be located in several rows if desired.

INDUSTRIAL UTILITY

The invention can be utilized in electronic imaging systems to permit high resolution still images to be produced at low frame rates, while also allowing standard NTSC motion image signals to be produced by the same system. The invention is particularly applicable to commercial camcorder devices.

What is claimed is:

1. An electronic image sensor comprising:

a row and column array of photosensitive pixels for generating image pixel signals in response to incident radiation; a horizontal output register; and vertical transfer means for transferring the image pixel signals generated by the photosensitive pixels to the horizontal output register;

wherein the vertical transfer means includes pixel dumping means for selectively preventing the image pixel signals generated in at least one of the columns of each row of the array of photosensitive pixels from being transferred to the horizontal output register;

wherein the vertical transfer means includes a row and column array of vertical transfer registers and the pixel dumping means includes a plurality of charge clearing structures in each row of vertical transfer registers; and

wherein the charge clearing structures of each row of vertical transfer registers are offset in different columns from the charge clearing structures of all other rows of vertical transfer registers.

2. The electronic image sensor of claim 1, wherein the vertical transfer means further comprises charge parking means for temporarily storing signal charge from at least one of the columns of each row of the array of photosensitive pixels, wherein signal charge packets from multiple rows of the array are summed in the charge parking means.

3. The electronic image sensor of claim 1, wherein the horizontal output register includes first and second horizontal transfer registers.

4. The electronic image sensor of claim 1, further comprising an auxiliary horizontal output register, wherein the auxiliary horizontal output register has a shorter line length than the horizontal output register.

5. The electronic image sensor of claim 4, wherein the horizontal output register and the auxiliary horizontal output register each include first and second horizontal transfer registers.

6. The electronic image sensor of claim 1, wherein the row and column array of vertical transfer registers comprises at least four rows.

7. An electronic imaging system comprising:

an electronic imaging sensor; an optical system for imaging scene light onto the electronic imaging sensor; a camera control processor coupled to the electronic imaging sensor; an operator control unit coupled to the camera control processor; and an image data storage unit coupled to the output of the electronic imaging sensor;

wherein the camera control processor controls the electronic imaging sensor to operate in either a still image mode or a motion image mode in response to a mode signal received from the operator control unit;

wherein the electronic imaging sensor comprises a row and column array of photosensitive pixels for generating image pixel signals in response to incident radiation, a horizontal output register, and vertical transfer means for transferring the image pixel signals generated by the photosensitive pixels to the horizontal output register, said vertical transfer means including pixel dumping means for selectively preventing the image pixel signals generated in at least one of the columns of each row of the array of photosensitive pixels from being transferred to the horizontal output register;

wherein the vertical transfer means includes a row and column array of vertical transfer registers and the pixel dumping means includes a plurality of charge clearing structures in each row of vertical transfer registers; and

wherein the charge clearing structures of each row of vertical transfer registers are offset in different columns from the charge clearing structures of all other rows of vertical transfer registers.

8. The electronic imaging system of claim 7, wherein the vertical transfer means further comprises charge parking means for temporarily storing signals from at least one of the columns of each row of the array of pixels, wherein signals from multiple rows of the array are summed in said charge parking means.

9. The electronic imaging system of claim 7, wherein the horizontal output register includes first and second horizontal transfer registers.

10. The electronic imaging system of claim 7, further comprising an auxiliary horizontal output register, wherein the auxiliary horizontal output register has a shorter line length than the horizontal output register.

11. The electronic imaging system of claim 10, wherein the horizontal output register and the auxiliary horizontal output register each include first and second horizontal transfer registers.

12. The electronic imaging system of claim 7, wherein the row and column array of vertical transfer registers comprises at least four rows.

* * * * *

EXHIBIT 44

US006697107B1

(12) **United States Patent**
Hamilton, Jr. et al.

(10) **Patent No.: US 6,697,107 B1**
(45) **Date of Patent: Feb. 24, 2004**

(54) **SMOOTHING A DIGITAL COLOR IMAGE USING LUMINANCE VALUES**

(75) Inventors: **John F. Hamilton, Jr.**, Rochester, NY (US); **James E. Adams, Jr.**, Rochester, NY (US)

(73) Assignee: **Eastman Kodak Company**, Rochester, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/112,554**

(22) Filed: **Jul. 9, 1998**

(51) **Int. Cl.**[7] **H04N 9/68**; H04N 5/208; H04N 5/21; G06K 9/40

(52) **U.S. Cl.** **348/234**; 348/252; 348/631; 382/264; 382/266

(58) **Field of Search** 348/235, 624, 348/631, 252, 253, 272, 273, 234; 382/300, 264, 254, 260

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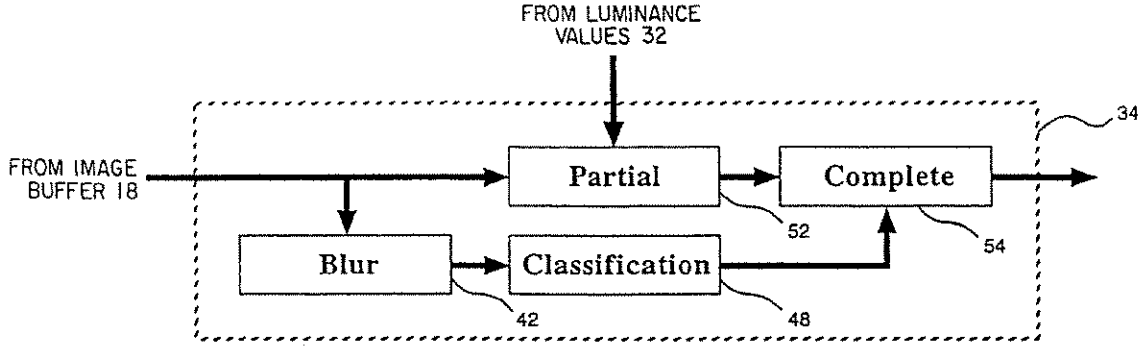
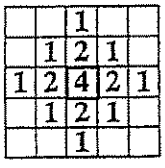
Primary Examiner—Wendy R. Garber
Assistant Examiner—Lin Ye
(74) *Attorney, Agent, or Firm*—Raymond L. Owens

(57) **ABSTRACT**

A method for smoothing a digital color image having color pixels in which each colored pixel is expressed as one luminance and two chrominance color values, including computing parameters for at least two orientations for each pixel in the stored digital image; using the computed parameters to form a classifier value for each such orientation and using such classifiers to determine the pixel classification based on such classifiers; and smoothing pixel chroma values according to the determined pixel classification.

10 Claims, 6 Drawing Sheets





/ 20

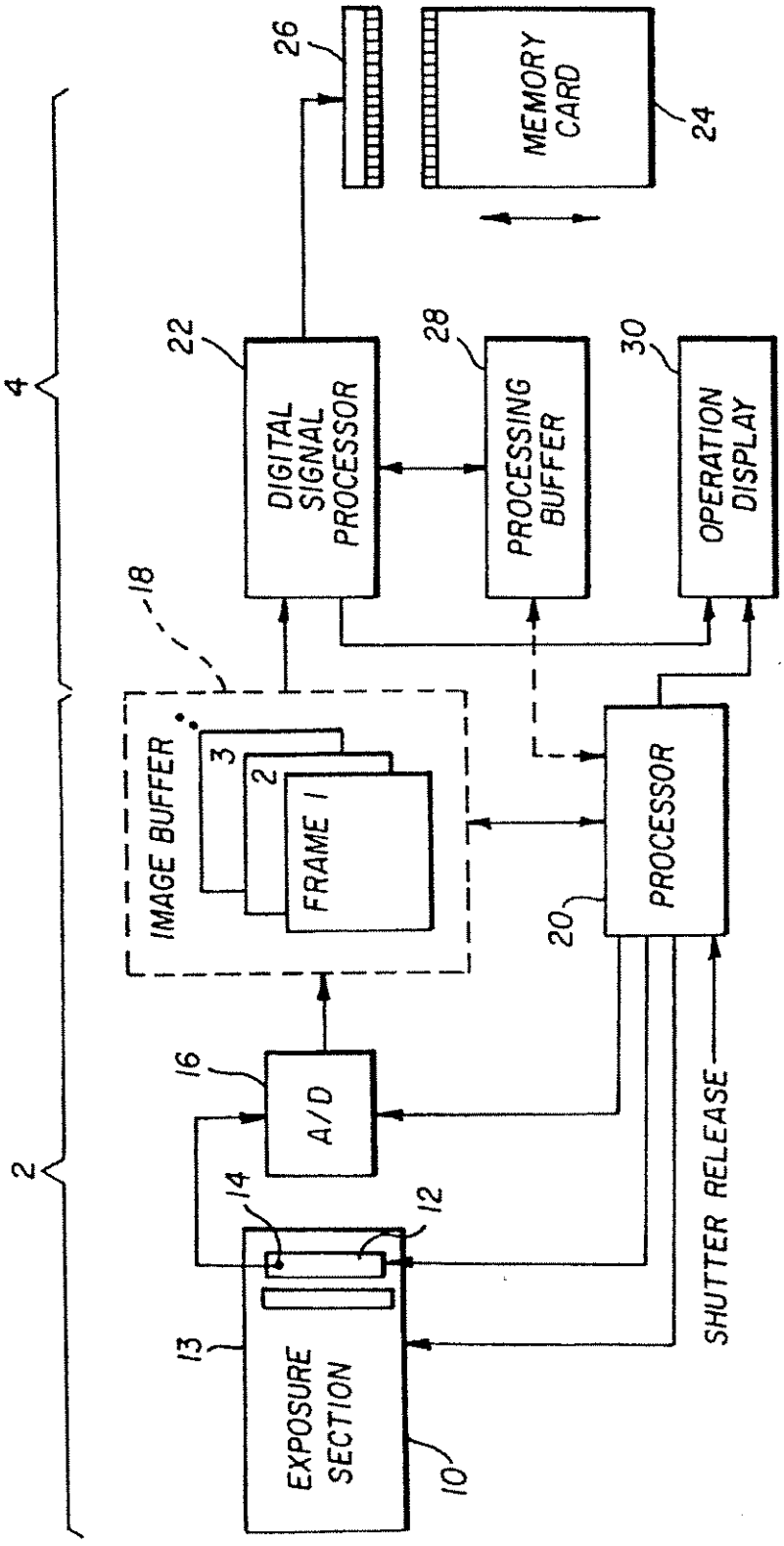


FIG. 1
(PRIOR ART)

AXD024534

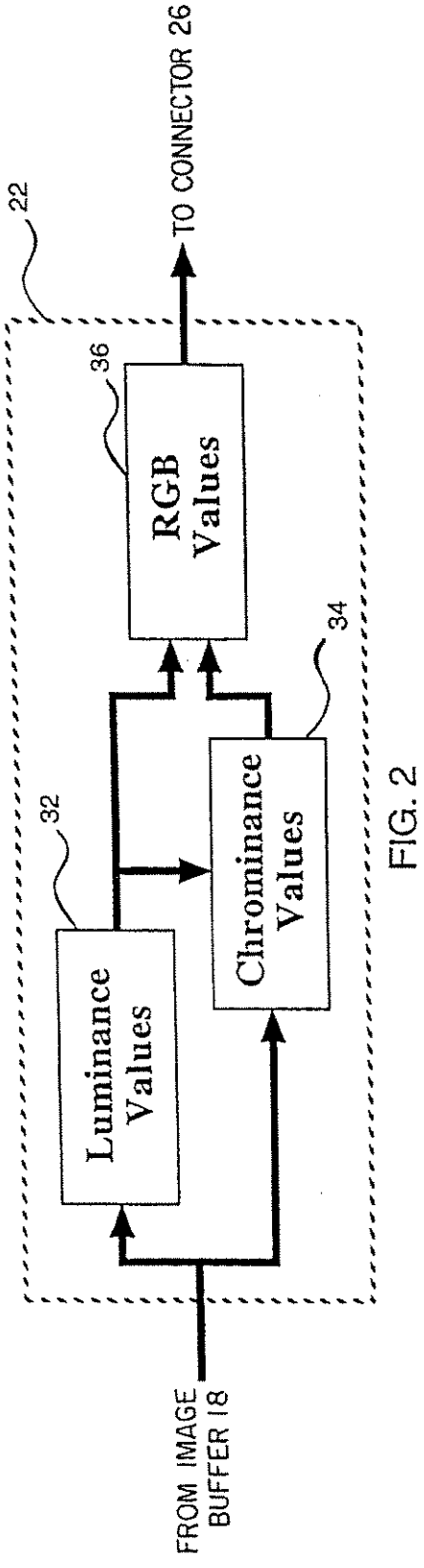

TO CONNECTOR 26
22
36
RGB Values
34
Chrominance Values
32
Luminance Values
FROM IMAGE BUFFER 18

FIG. 2

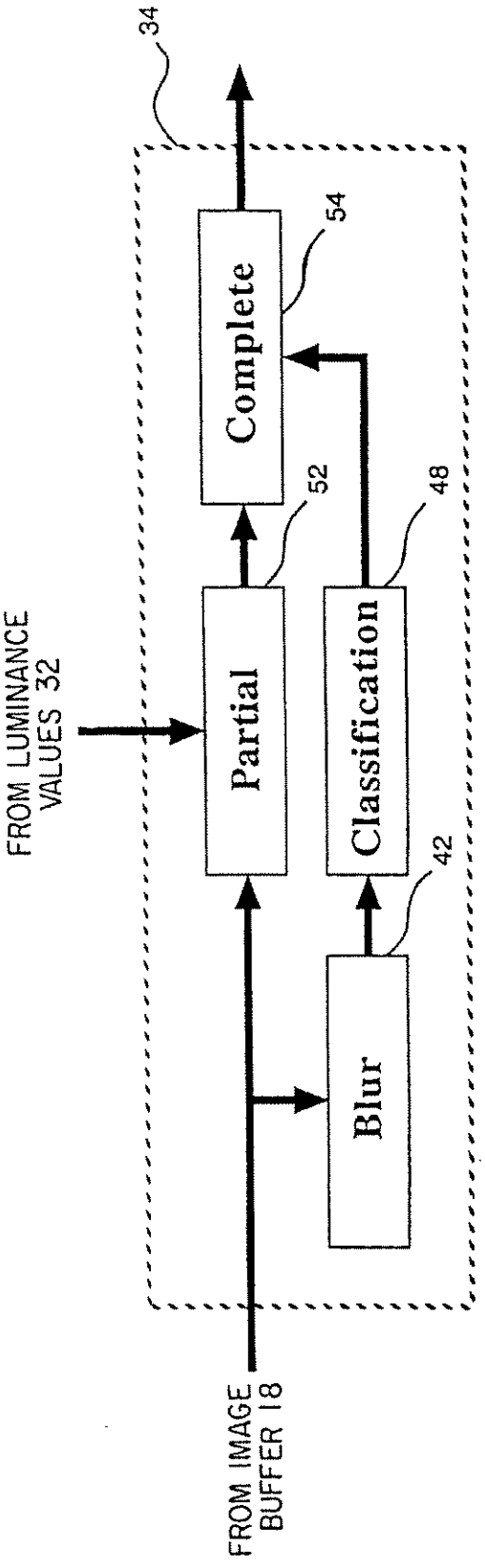

34
Complete
54
52
48
Partial
Classification
42
Blur
FROM LUMINANCE VALUES 32
FROM IMAGE BUFFER 18

FIG. 3

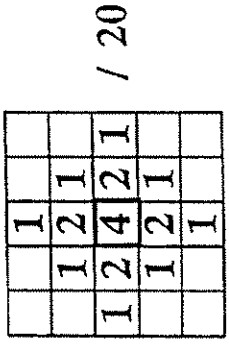

/ 20
1 1 2 1
1 2 4 2 1
1 2 1 1
1 2 1
1

FIG. 4

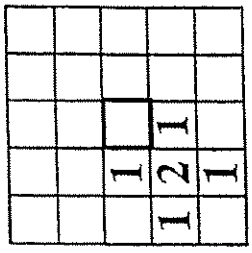


FIG. 5C

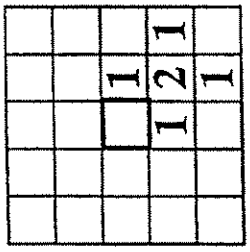


FIG. 6C

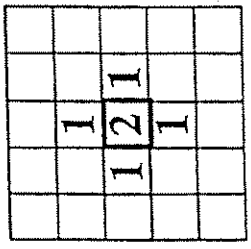


FIG. 5B

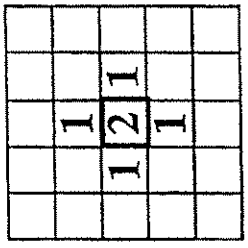


FIG. 6B

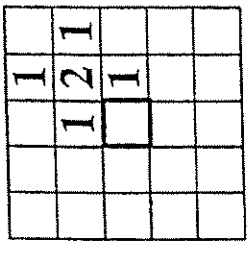


FIG. 5A

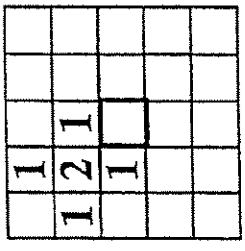


FIG. 6A

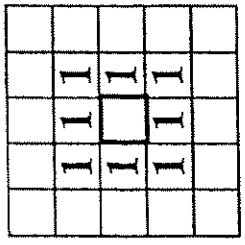


FIG. 7C

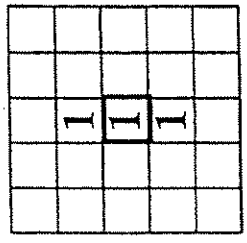


FIG. 7B

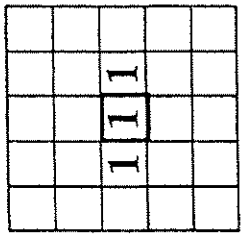


FIG. 7A

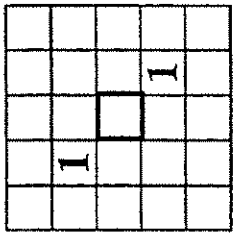


FIG. 7E

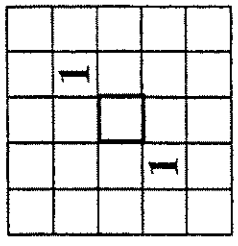


FIG. 7D

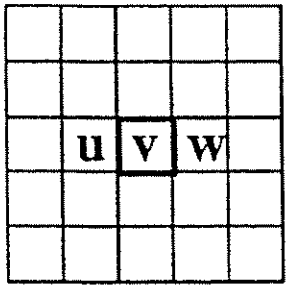


FIG. 8A

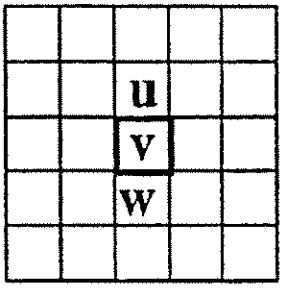


FIG. 8B

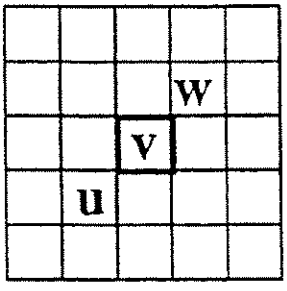


FIG. 8C

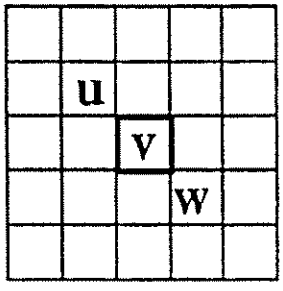


FIG. 8D

SMOOTHING A DIGITAL COLOR IMAGE USING LUMINANCE VALUES

CROSS REFERENCE TO RELATED APPLICATIONS

Reference is made to commonly assigned U.S. patent application Ser. No. 09/096,632, filed Jun. 12, 1998, entitled "Computing Color Specification (Luminance and Chrominance) Values for Images" to John F. Hamilton, Jr. et al., the disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates to digital color image processing and, more particularly, to smoothing the digital color image.

BACKGROUND OF THE INVENTION

With the advent of digital cameras, it is becoming more and more advantageous to capture images as colored digital images. Colored digital images are frequently stored in three color planes such as red, green, and blue, or cyan, magenta, and yellow. In image processing, these colored digital images luminance and chrominance color coordinates are quite useful because they express color in a similar fashion to the way the human visual system operates. As is well known, luminance, the black and white portion of an image, determines the sharpness of such image while the chrominance values determines its colorfulness.

As also is well known to those skilled in the art, generally three channels are used to describe a color. For example, if an image is recorded having red, green, and blue channels, this can be converted to one luminance channel and two chrominance channels such as Y, Cr, Cb. These luminance and two chrominance channels facilitate certain aspects of digital image processing. Color interpolation between pixels can reduce the noise level in the luminance channel, but not without the expense of increasing noise in the chrominance channel. If this noise if left untreated, artifacts can appear in an output image which often are characterized by being splotchy in appearance.

This splotchy color problem can be reduced by smoothing the chrominance channels. Because the chrominance content of the images is usually of low spatial frequency and the noise content is of high spatial frequency, the application of a low-pass blur filter has been found to reduce noise levels without significantly reducing image quality. However, the higher the noise level, the more aggressive the smoothing or blurring should be.

A problem with chrominance smoothing occurs at the edges in a digital image. If the blurring is aggressive (passing lower frequencies) and the colors near the edge are bold (have high chroma), the blurring will cause the colors to "bleed" across the edge. In this situation, the image around the edge is easily seen by a viewer to be unnatural.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an effective way of smoothing digital color images which minimizes the problem of color bleeding across image edges discussed above.

This object is achieved by a method for smoothing a digital color image having color pixels in which each colored pixel is expressed as one luminance and two chrominance color values, such method comprising the steps of:

a) computing parameters for at least two orientations for each pixel in the stored digital image;

b) using the computed parameters to form a classifier value for each such orientation and using such classifiers to determine the pixel classification based on such classifiers; and

c) smoothing pixel chroma values according to the determined pixel classification.

ADVANTAGES

An advantage of the present invention is the recognition that chroma values can be corrected in accordance with the present invention to provide highly effective smoothing of digital color image.

Another advantage of the present invention is that it greatly reduced color bleeding across edges. The method can be readily implemented and assigns each pixel to one of five classes which are used in color smoothing. This invention readily lends itself to digital image processing.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of an electronic still camera employing interpolation processing according to the invention;

FIG. **2** is a block diagram of the logic of the interpolation processing technique for producing luminance in accordance with the invention;

FIG. **3** shows a detailed block diagram of the chrominance values block **34** shown in FIG. **2**;

FIG. **4** depicts a kernel used in computing low frequency luminance values;

FIGS. **5**A–C depict pixel weights used in computing a classifier in the classification block **48** shown in FIGS. **3**A and **3**B;

FIGS. **6**A–C also depict pixel weights used in computing another classifier produced by the classification block **48**;

FIGS. **7**A–**7**E respectively show the kernel weights for smoothing (i.e. blurring) chrominance for pixels which have been classified as horizontal, vertical, flat, diag**1**, and diag**2**; and

FIGS. **8**A–D respectively show horizontal, vertical, diag**1**, and diag**2** orientations when no CFA data are available.

DETAILED DESCRIPTION OF THE INVENTION

Single-sensor electronic cameras employing color filter arrays are well known. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. **1** and **2**, an electronic still camera **1** is divided generally into an input section **2** and an interpolation and recording section **4**. The input section **2** includes an exposure section **10** for directing image light from a subject (not shown) toward an image sensor **12**. Although not shown, the exposure section **10** includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The image sensor **12**, which includes a two-dimensional array of colored photosites or pixels corresponding to picture elements of the image, can be a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. The image sensor **12** is covered by a color filter array (CFA) **13**. For an example of a color filter array which is particularly suitable for use in the present invention

reference is made to commonly-assigned U.S. Pat. No. 5,631,703 to Hamilton et al, the disclosure of which is incorporated by reference. The image sensor **12** is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode **14**, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter **16**, which generates a digital image value from the analog input signal for each picture element. The digital values are applied to an image buffer **18**, which may be a random access memory (RAM) with storage capacity for a plurality of still images.

A control processor **20** generally controls the input section **2** of the electronic still camera **1** by initiating and controlling exposure ((by operation by the diaphragm and shutter (not shown) in the exposure section **10**)), by generating the horizontal and vertical clocks needed for driving the image sensor **12** and for clocking image information therefrom, and by enabling the A/D converter **16** in conjunction with the image buffer **18** for each value segment relating to a picture element. The control processor **20** typically includes a microprocessor and appropriate memory coupled to a system timing circuit. Once a certain number of digital image values have been accumulated in the image buffer **18**, the stored values are applied to a digital signal processor **22**, which controls the throughput processing rate for the interpolation and recording section **4** of the electronic still camera **1**. The digital signal processor **22** applies an interpolation algorithm to the digital image values, and sends the interpolated values to a conventional, removable memory card **24** via a connector **26**. Although an electronic still camera **1** has been described as including a digital signal processor, it will be understood that the digital signal processor **22** does not have to be an integral part of the electronic still camera **1**. A requirement of this invention is that the digital image values are provided from an image sensor.

Since the interpolation and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer **28**. The processing buffer **28** may also be configured as part of the memory space of the image buffer **18**. The number of image values needed in the image buffer **18** before digital processing can begin depends on the type of processing, that is, for a neighborhood interpolation to begin, a block of values including at least a portion of the image values comprising a video frame must be available. Consequently, in most circumstances, the interpolation may commence as soon as the requisite block of picture elements is present in the buffer **18**.

The input section **2** operates at a rate commensurate with normal operation of the electronic still camera **1** while interpolation, which may consume more time, can be relatively divorced from the input rate. The exposure section **10** exposes the image sensor **12** to image light for a time period dependent upon exposure requirements, for example, a time period between $\frac{1}{1000}$ second and several seconds. The image charge is then swept from the photosites in the image sensor **12**, converted to a digital format, and written into the image buffer **18**. The driving signals provided by the control processor **20** to the image sensor **12**, the A/D converter **16** and the buffer **18** are accordingly generated to achieve such a transfer. The processing throughput rate of the interpolation and recording section **4** is determined by the speed of the digital signal processor **22**.

One desirable consequence of this architecture is that the processing algorithm employed in the interpolation and recording section may be selected for quality treatment of the image rather than for throughput speed. This, of course, can put a delay between consecutive pictures which may affect the user, depending on the time between photographic events. This is a problem since it is well known and understood in the field of electronic imaging that a digital still camera should provide a continuous shooting capability for a successive sequence of images. For this reason, the image buffer **18** shown in FIG. **1** provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. The size of the buffer is established to hold enough consecutive images to cover most picture-taking situations.

An operation display panel **30** is connected to the control processor for displaying information useful in operation of the electronic still camera **1**. Such information might include typical photographic data, such as shutter speed, aperture, exposure bias, color balance (auto, tungsten, fluorescent, daylight), field/frame, low battery, low light, exposure modes (aperture preferred, shutter preferred), and so on. Moreover, other information unique to this type of electronic still camera **1** is displayed. For instance, the removable memory card **24** would ordinarily include a directory signifying the beginning and ending of each stored image. This would show on the display panel **30** as either (or both) the number of images stored or the number of image spaces remaining, or estimated to be remaining.

The digital signal processor **22** interpolates each still video image stored in the image buffer **18** according to the interpolation technique shown in FIG. **2**. The interpolation of missing data values at each pixel location follows the sequence shown in FIG. **2**, as will later be discussed.

In the implementation shown in FIG. **2**, the digital signal processor **22** provides an adaptive interpolation technique to provide a compute luminance function shown as luminance values block **32** for computing luminance values as will be described hereinafter in connection with FIG. **3**. After the luminance values are computed then a chrominance values block **34** computes the chrominance values of each pixel based upon the computed final luminance values. Finally an RGB values block **36** computes the image in Red(R), Green(G), Blue(B) format which are used for an image display or for making a hard copy output. Although this disclosure is in reference to computing red, green, and blue values, it will be understood that it is also applicable to other color spaces such as cyan, magenta, and yellow. Another color space that can be used is to use luminance and chrominance values which are typically referred to as YCC color spaces. The Y refers to luminance and the two C's refer to chrominance. Luminance values are computed as shown in FIG. **2** in the digital signal processor of FIG. **1** as is well known in the art. For a more complete description of the computation of such luminance values, reference can be made to commonly assigned U.S. patent application Ser. No. 09/096,632, filed Jun. 12, 1998, entitled "Computing Color Specification (Luminance and Chrominance) Values for Images" to John F. Hamilton, Jr. et al.

Turning now to FIG. **3**, the chrominance values block **34** is shown in more detail. Beginning with the details of blur block **42**, reference is made to FIG. **4** where a 5×5 blur kernel arrangement is shown. For any given pixel which is selected as the center pixel of a 5×5 kernel it is assigned value weight of 4. Pixels which surround the kernel of interest are also assigned different values. These values shown in FIG. **4** are representative and those skilled in the art will appreciate that other values can be selected which will also provide an appropriate blur function. Note that

once the weighted sum is computed is divided by 20, which is the sum of all the weights in the blur kernel. The following equations depict how these kernel values are used to compute each pixel in a digital image which has high frequency components removed.

If the recorded CFA color values are:

$$\begin{matrix} A_{11} & A_{12} & A_{13} & A_{14} & A_{15} \\ A_{21} & A_{22} & A_{23} & A_{24} & A_{25} \\ A_{31} & A_{32} & A_{33} & A_{34} & A_{35} \\ A_{41} & A_{42} & A_{43} & A_{44} & A_{45} \\ A_{51} & A_{52} & A_{53} & A_{54} & A_{55} \end{matrix}$$

then the following equations show how the blur kernel values of FIG. 4 are used to produce the blurred luminance value B_{33} for the center pixel above.

$$B_{33} = (1*A_{13} + 1*A_{22} + 2*A_{23} + 1*A_{24} + 1*A_{31} + 2*A_{32} + 4*A_{33} + 2*A_{34} + 1*A_{35} + 1*A_{42} + 2*A_{43} + 1*A_{44} + 1*A_{53})/20$$

The output of blur block 42 is applied to classification block 48. The computation provided by classification block 48 will now be described.

If the blurred luminance values are:

$$\begin{matrix} B_{11} & B_{12} & B_{13} & B_{14} & B_{15} \\ B_{21} & B_{22} & B_{23} & B_{24} & B_{25} \\ B_{31} & B_{32} & B_{33} & B_{34} & B_{25} \\ B_{41} & B_{42} & B_{43} & B_{44} & B_{45} \\ B_{51} & B_{52} & B_{53} & B_{54} & B_{55} \end{matrix}$$

then the following equations show how the horizontal (horz) and vertical (vert) classifiers are computed for the center pixel.

$$\text{horz}=\text{Abs}(u-w)+\text{Abs}(u-2*v+w)$$

where

the term (u−w) is a gradient value,

the term (u−2*v+w) is a Laplacian second-order value,

$u=B_{31}$,

$v=B_{33}$,

$w=B_{35}$.

$$\text{vert}=\text{Abs}(u-w)+\text{Abs}(u-2*v+w)$$

where

$u=B_{13}$,

$v=B_{33}$,

$w=B_{53}$.

The two diagonal orientations will be named diag1 and diag2 and correspond to a diagonal line of slope 1 (connecting lower left to upper right) and a diagonal line of slope −1 (connecting upper left to lower right) respectively. The classifiers for diag1 and diag2 are computed using the kernel values shown in FIGS. 5A–5C and FIGS. 6A–6C respectively. The classifier equations using said kernel values are as follows:

$$\text{diag1}=(\text{Abs}(u-w)+\text{Abs}(u-2*v+w))/3$$

where

$$u = (1*B_{14} + 1*B_{23} + 2*B_{24} + 1*B_{25} + 1*B_{34})$$

$$v = (1*B_{23} + 1*B_{32} + 2*B_{33} + 1*B_{34} + 1*B_{43})$$

$$w = (1*B_{32} + 1*B_{41} + 2*B_{42} + 1*B_{43} + 1*B_{52})$$

and

$$\text{diag2}=(\text{Abs}(u-w)+\text{Abs}(u-2*v+w))/3$$

where

$$u = (1*B_{12} + 1*B_{21} + 2*B_{22} + 1*B_{23} + 1*B_{32})$$

$$v = (1*B_{23} + 1*B_{32} + 2*B_{33} + 1*B_{34} + 1*B_{43})$$

$$w = (1*B_{34} + 1*B_{43} + 2*B_{44} + 1*B_{45} + 1*B_{54})$$

If a pixel's horizontal and vertical classifier are both less than a fixed threshold, such as 24, the pixel is classified as "flat" and the flat chrominance blur kernel is used (see FIG. 7C). Otherwise, a pixel's classification is determined by the smallest classifier which indicates the preferred orientation of interpolation such as horizontal, vertical, diag1, or diag2.

Initial chrominance values for the image are computed in partial block 52 and passed to complete block 54, where they are smoothed according to the selected pixel classification.

The chrominance blur kernels for the preferred orientations horizontal, vertical, diag1, and diag2 are shown in FIGS. 7A, 7B, 7D, and 7E, respectively. For a specific example, suppose the classifier values for horizontal, vertical, diag1, and diag2 were 32, 20, 18, and 25, respectively. Because the horizontal classifier 32 exceeds the threshold of 24, the pixel is not classified as "flat." So then the minimum value 18 being the diag1 classifier determines that the preferred direction for chrominance smoothing is diag1. Using the chrominance blur kernel weights for the diag1 orientation (FIG. 7D), the smoothed chrominance value C33 would be:

$$C_{33} = (A_{24} + A_{42})/2$$

The present invention can also be applied to images for which no CFA data is available. In this situation, the method of chrominance smoothing is the same except that the low-frequency luminance data used to classify each pixel comes from image luminance data rather than from original CFA data. The lower the noise content in the image luminance data, the lower the degree of luminance blurring required for robust pixel classification.

In the simplest case, the pixel classifiers would still be computed as before:

$$\text{Abs}(u-w)+\text{Abs}(u-2v+w)$$

But, the values for u, v, and w would be single nearby luminance values as shown in FIGS. 8A–D, respectively, for the horizontal, vertical, diag1, and diag2 orientations. Stated differently, the values u, v, and w are not weights in this case but are the actual luminance values. The pixel of interest is shown for convenience as the central pixel and these views show the relative location, with respect to the central pixel, of the values u, v, and w.

The present invention can be embodied in a computer program stored on a computer readable product such as, for

example, magnetic storage media, such as a magnetic disk (for example, a floppy disk), magnetic tape, optical disks, optical tape, or machine readable memory.

The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

PARTS LIST

2	input section
4	recording section
10	exposure section
12	image sensor
13	color filter array
14	output diode
16	A/D converter
18	image buffer
20	control processor
22	digital signal processor
24	removable memory card
26	connector
28	processing buffer
30	display panel
32	luminance values block
34	chrominance values block
36	RGB values
42	blur block
48	classification block
52	partial block
54	complete block

What is claimed is:

1. A method for smoothing a digital color image having color pixels in which each colored pixel is expressed as one luminance (Y) and two chrominance (Cr,Cb) color values, such method comprising:

computing parameters for at least two orientations for each existing pixel in the stored digital image where each colored pixel is expressed as the one luminance (Y) and two chrominance (Cr,Cb) color values;

using the computed parameters to form a classifier value for each such orientation and using such classifiers to determine the pixel classification based on such classifiers; and

smoothing the pixel chrominance (Cr,Cb) color values of each existing pixel according to the determined pixel classification.

2. A method for smoothing a digital color image having color pixels in which each colored pixel is expressed as one luminance (Y) and two chrominance (Cr,Cb) color values, such method comprising:

determining a luminance gradient and Laplacian for each of at least two orientations for each existing pixel in the stored digital image where each pixel is expressed as the one luminance (Y) and two chrominance (Cr,Cb) color values;

combining the gradient and Laplacian to form a classifier value for each such orientation and using such classifiers to determine the pixel classification based on such classifiers; and

smoothing the pixel chrominance (Cr,Cb) color values of each existing pixel according to the determined pixel classification.

3. The method of claim 2 wherein there are four classifiers each having a value associated with each pixel which are horizontal, vertical, slope 1 diagonal, and slope −1 diagonal.

4. The method of claim 2 further including comparing the horizontal and vertical classifiers to determine if they are less than a predetermined threshold and, if so, classifying the pixel as having a flat orientation, but when above such threshold, classifying according to the smallest classifier value and using such selected orientation to perform smoothing.

5. The method of claim 2 wherein the pixel classification is a function only of neighboring luminance pixel values.

6. An apparatus for processing a digital color image having color pixels in which each colored pixel is expressed as one luminance (Y) and two chrominance (Cr,Cb) color values, such apparatus comprising:

means for storing the pixels of the digital color image where each pixel is expressed as the one luminance (Y) and two chrominance (Cr,Cb) color values; and

processor means operatively associated with the storage means and responsive to the stored luminance values for obtaining Laplacian second-order and gradient values in at least two image orientations including:

means for combining the Laplacian second-order and the gradient values to define a classifier for each image orientation at each existing image pixel to determine a preferred orientation for smoothing from the set of classifier values at each pixel; and

means responsive to the determined preferred orientation for smoothing both the stored chrominance (Cr,Cb) color values for each existing corresponding image pixel.

7. The apparatus of claim 6 wherein there are four classifiers each having a value associated with each pixel which are horizontal, vertical, slope 1 diagonal, and slope −1 diagonal.

8. The apparatus of claim 6 further including comparing the horizontal and vertical classifiers to determine if they are less than a predetermined threshold and, if so, classifying the pixel as having a flat orientation, but when above such threshold, classifying according to the smallest classifier value and using such selected orientation to perform smoothing.

9. The apparatus of claim 6 wherein the pixel classification is a function only of neighboring luminance pixel values.

10. A computer program product for processing a stored digital color image having color pixels in which each colored pixel is expressed as one luminance (Y) and two chrominance (Cr,Cb) color values, comprising:

a computer readable storage medium including programming means, processor means operatively associated with storage storing the pixels of the digital color image where each pixel is expressed as the one luminance (Y) and two chrominance (Cr,Cb) color values and responsive to the stored luminance values for obtaining Laplacian second-order and gradient values in at least two image orientations including:

means for combining the Laplacian second-order and the gradient values to define a classifier for each image orientation at each existing image pixel to determine a preferred orientation for smoothing from the set of classifier values at each pixel; and

means responsive to the determined preferred orientation for smoothing and the stored chrominance values for smoothing both chrominance color values for each existing corresponding image pixel.

* * * * *

EXHIBIT 45

United States Patent [19]

Vogel

[11] **Patent Number: 4,714,963**

[45] **Date of Patent: Dec. 22, 1987**

[54] **ASYNCHRONOUS STILL TIMING FOR A VIDEO CAMERA PRODUCING MOVIE OR STILL IMAGES**

[75] Inventor: **Richard M. Vogel**, Rochester, N.Y.

[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[21] Appl. No.: **882,121**

[22] Filed: **Jul. 3, 1986**

[51] **Int. Cl.**[4] **H04N 3/14**

[52] **U.S. Cl.** **358/213.26**; 358/213.31; 358/909

[58] **Field of Search** 358/909, 213.31, 213.26, 358/213.19, 335, 228

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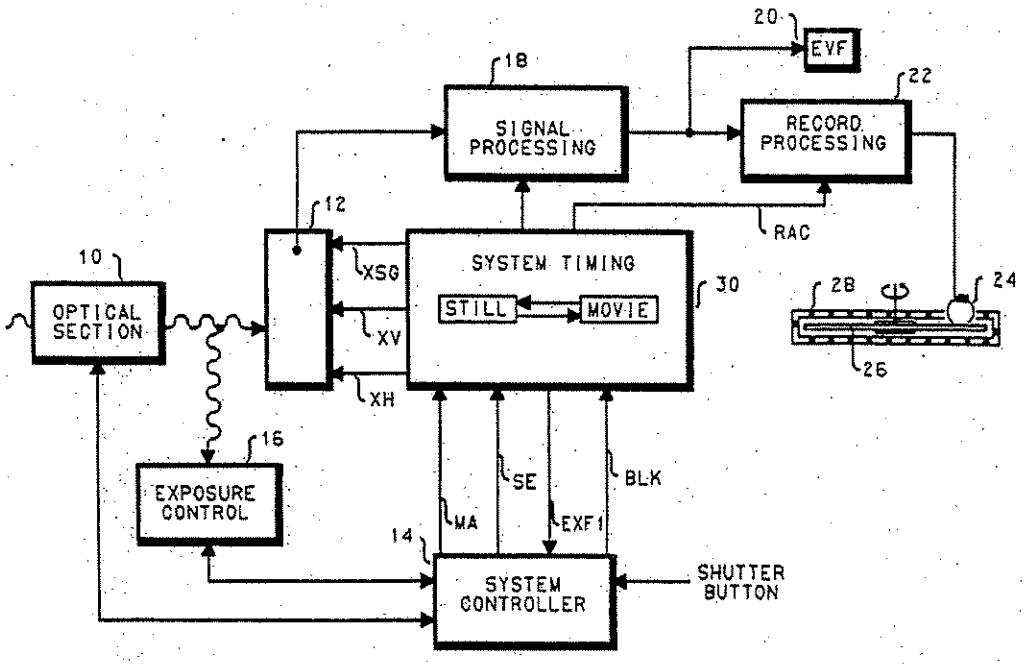
Primary Examiner—Gene Z. Rubinson
Assistant Examiner—Stephen Brinich
Attorney, Agent, or Firm—David M. Woods

[57] **ABSTRACT**

A still video camera produces a movie image for previewing in an electronic viewfinder according to a specific image repetition rate and a still image for recording on a magnetic disk. In the movie mode, video signals are clocked from a solid-state, interline transfer image sensor by application of driving signals from a movie timing generator. The still mode interrupts the movie timing with a special driving signal from a still timing generator. By initiating the still exposure in synchronism with the high frequency movie driving signals that operate the image sensor . . . and not with regard to the vertical drive interval determining the image repetition rate . . . a "pseudo"-asynchronous relationship can be obtained with the movie mode and the still exposure can begin without noticeable delay. After the still exposure is completed, control of the image sensor is returned to the movie timing generator in synchronism with the image repetition rate.

11 Claims, 9 Drawing Figures



AXD024477

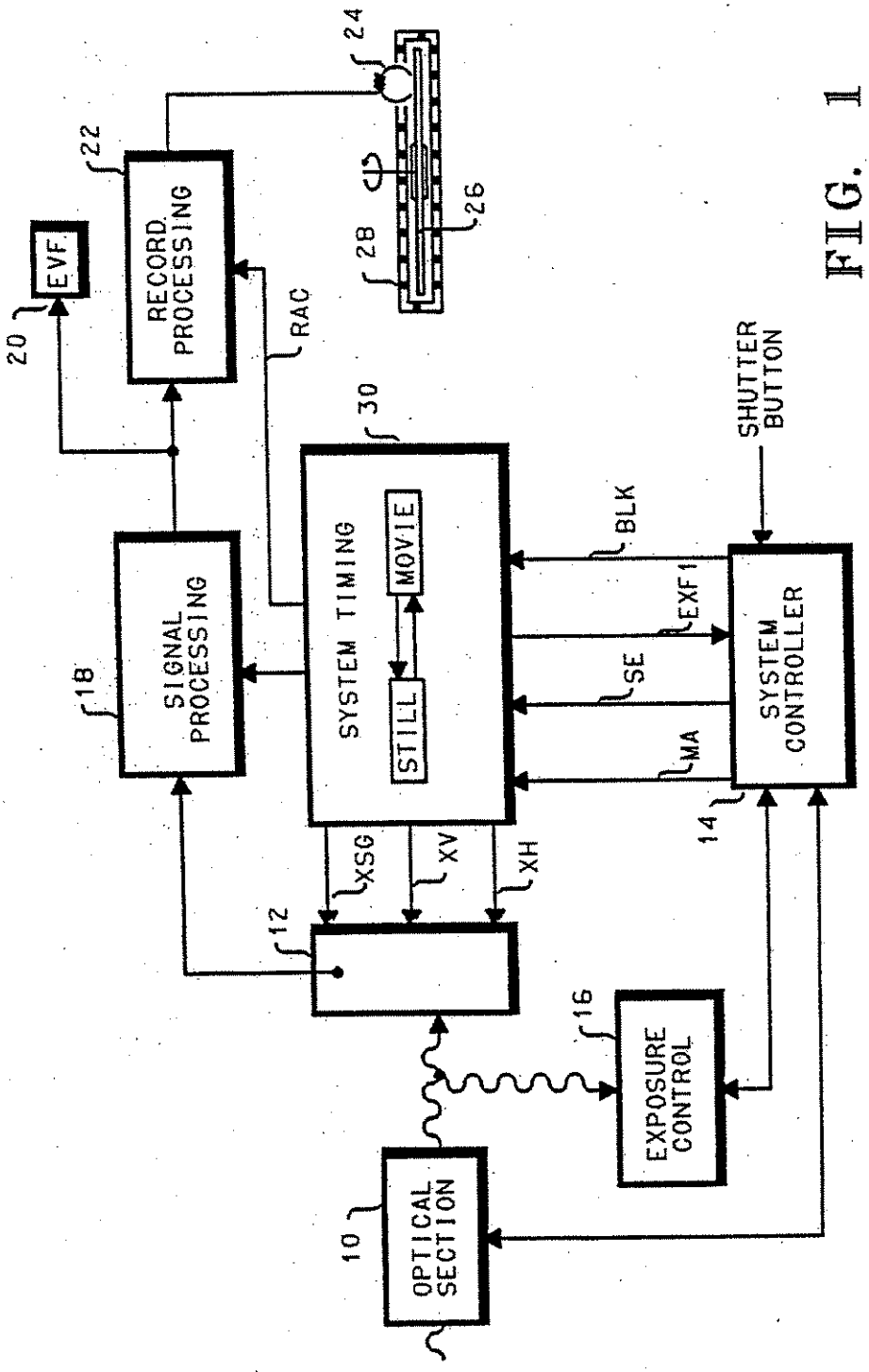


FIG. 1

AXD024478

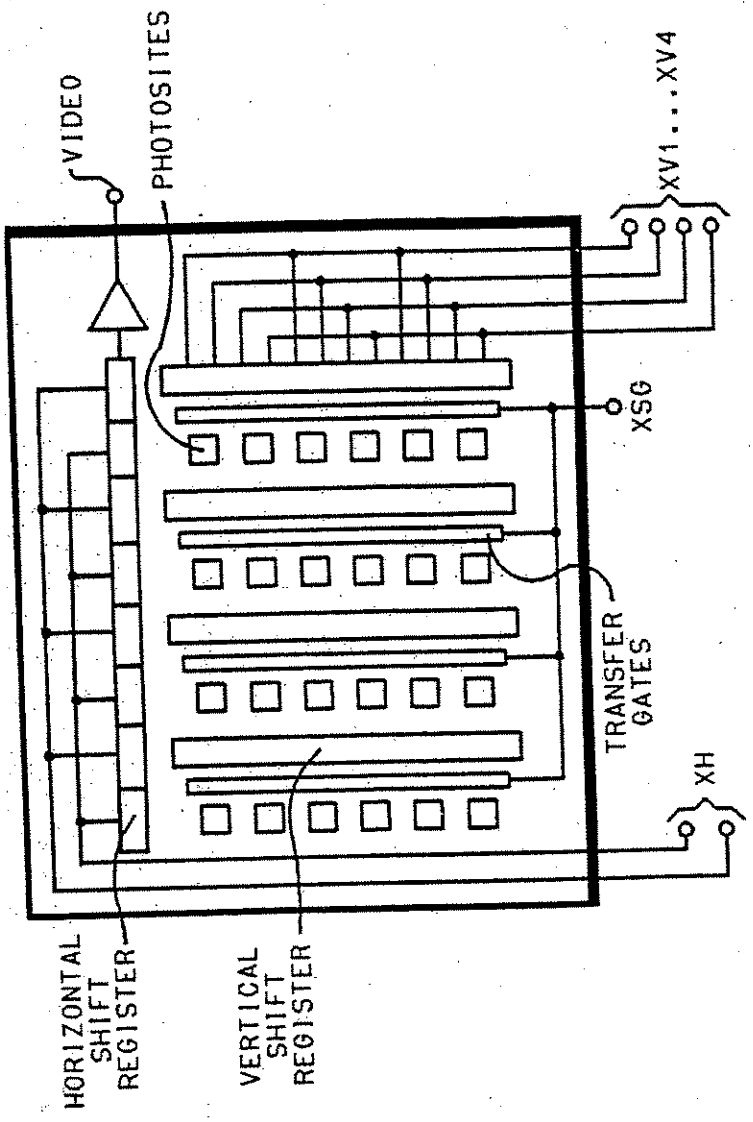

VIDEO
PHOTOSITES
XV1...XV4
XSG
TRANSFER GATES
XH
HORIZONTAL SHIFT REGISTER
VERTICAL SHIFT REGISTER

FIG. 2

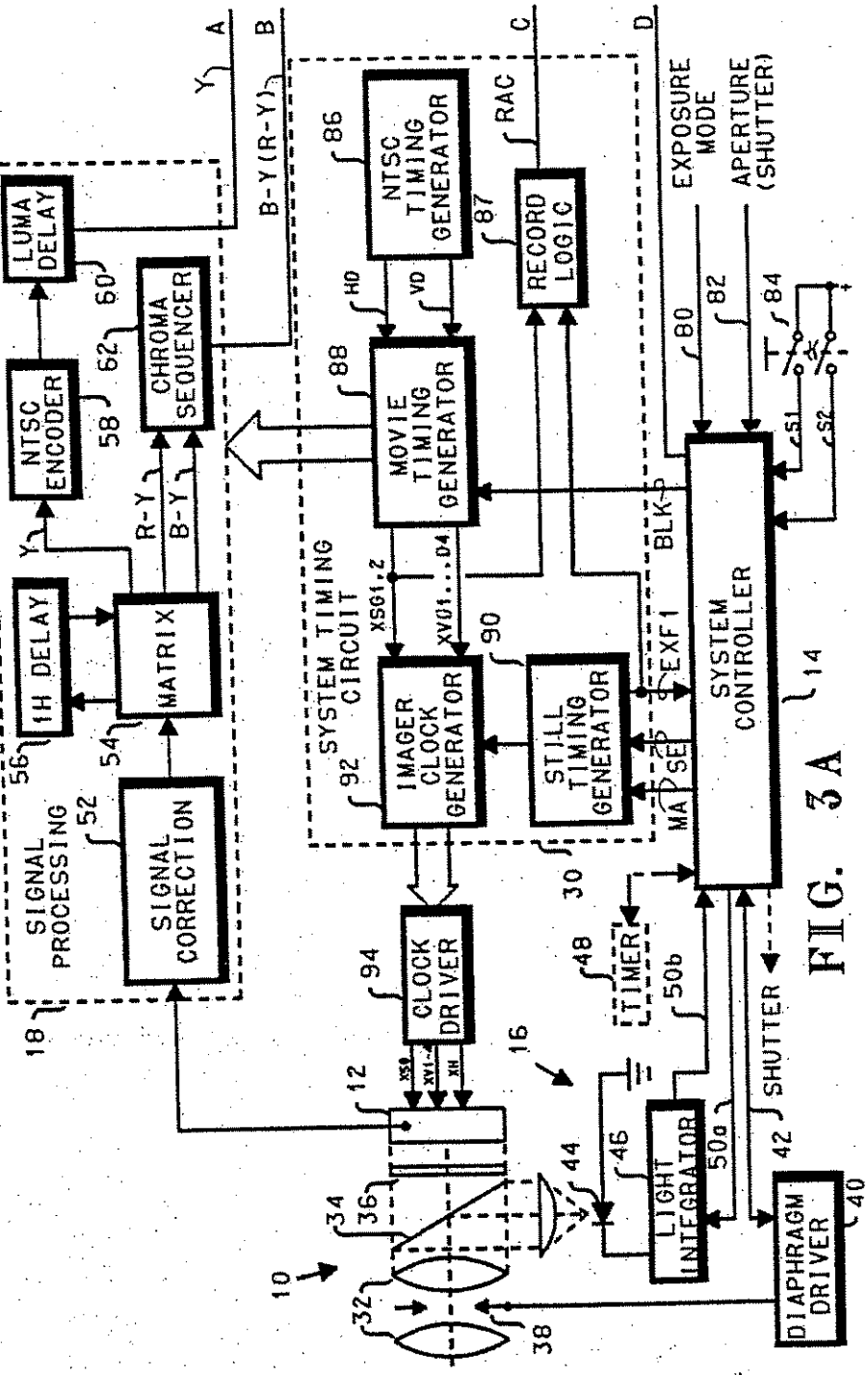

A
B
C
D
Y
B-Y(R-Y)
RAC
EXPOSURE MODE
APERTURE (SHUTTER)
LUMA DELAY
NTSC TIMING GENERATOR
RECORD LOGIC
CHROMA SEQUENCER
NTSC ENCODER
MOVIE TIMING GENERATOR
1H DELAY
MATRIX
SYSTEM TIMING CIRCUIT
IMAGER CLOCK GENERATOR
STILL TIMING GENERATOR
SYSTEM CONTROLLER
SIGNAL PROCESSING
SIGNAL CORRECTION
CLOCK DRIVER
TIMER
LIGHT INTEGRATOR
DIAPHRAGM DRIVER
SHUTTER
R-Y
B-Y
BLK
EXF1
MASE
HD
VD
XS61,2
XV01...04
XS
XV1-4
XH
10
12
14
16
18
30
32
34
36
38
40
42
44
46
48
50a
50b
52
54
56
58
60
62
80
82
84
86
87
88
90
92
94
S1
S2

FIG. 3A

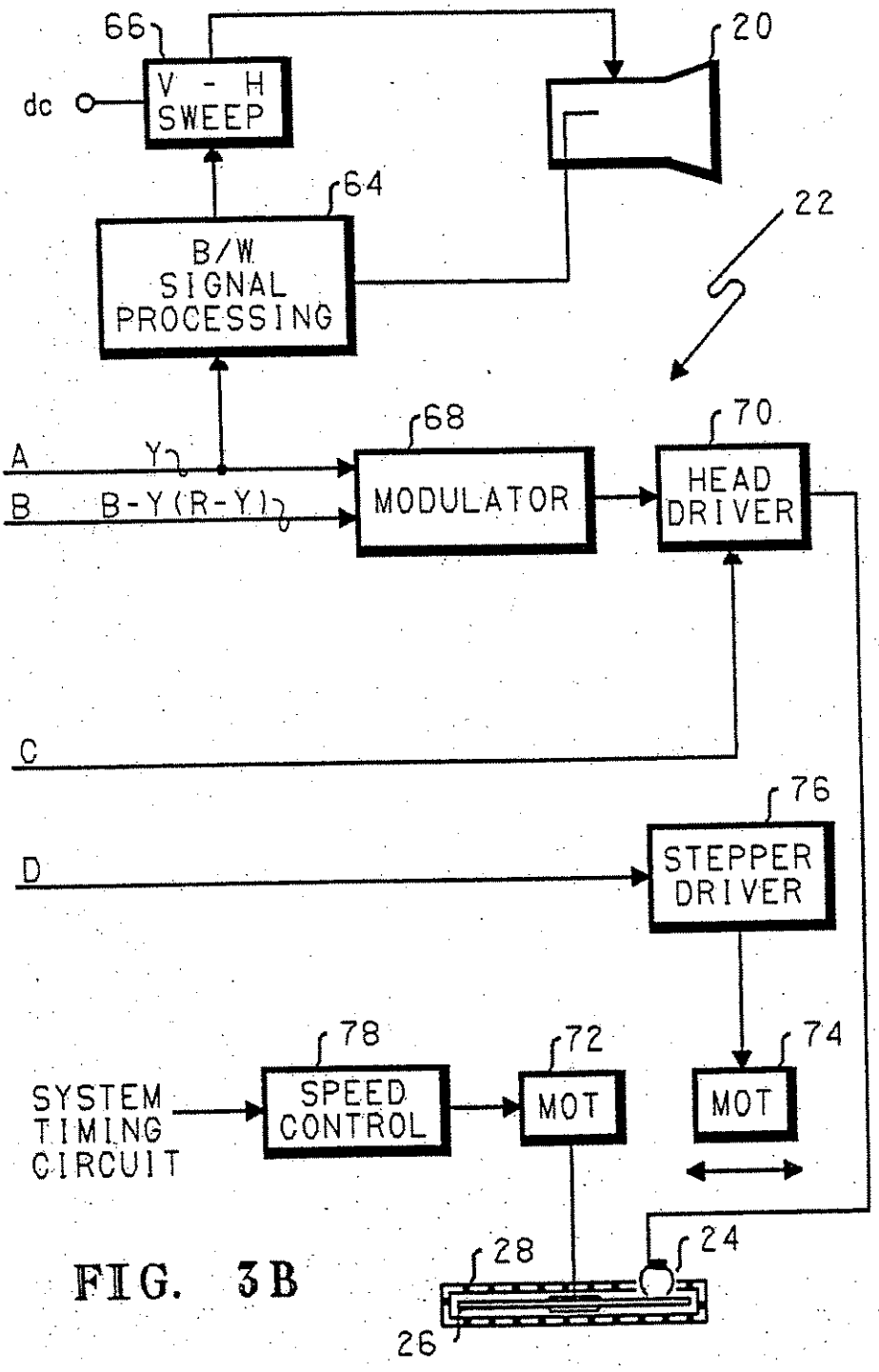

66
V - H SWEEP
dc
20
64
B/W SIGNAL PROCESSING
22
68
70
A
Y
B
B-Y(R-Y)
MODULATOR
HEAD DRIVER
C
76
D
STEPPER DRIVER
78
72
74
SYSTEM TIMING CIRCUIT
SPEED CONTROL
MOT
MOT
28
24
26

FIG. 3B

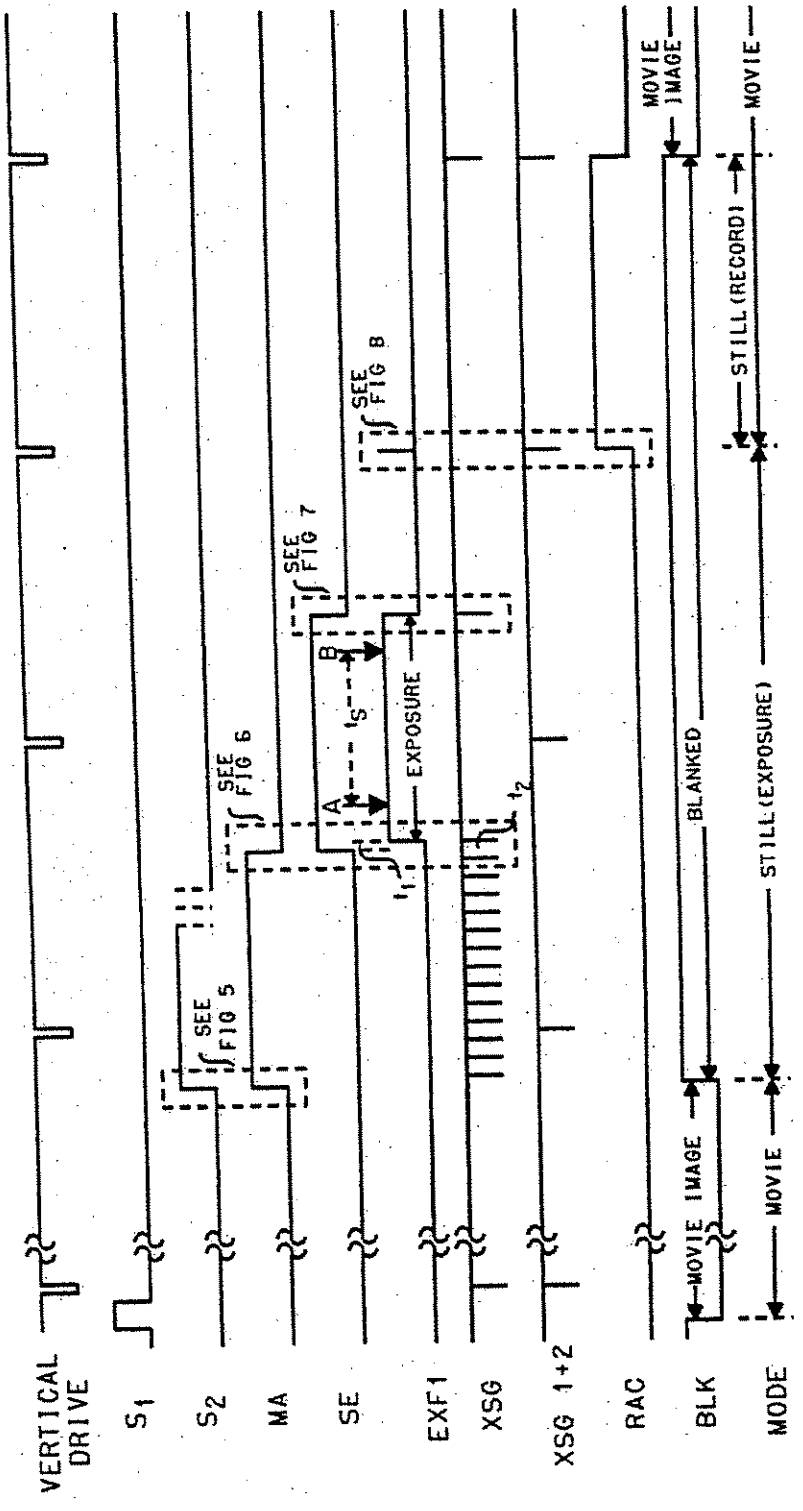

VERTICAL DRIVE
S1
S2
MA
SE
EXF1
XSG
XSG 1+2
RAC
BLK
MODE
SEE FIG 5
SEE FIG 6
SEE FIG 7
SEE FIG 8
EXPOSURE
BLANKED
MOVIE IMAGE
STILL (RECORD)
STILL (EXPOSURE)
MOVIE
A
B

FIG. 4

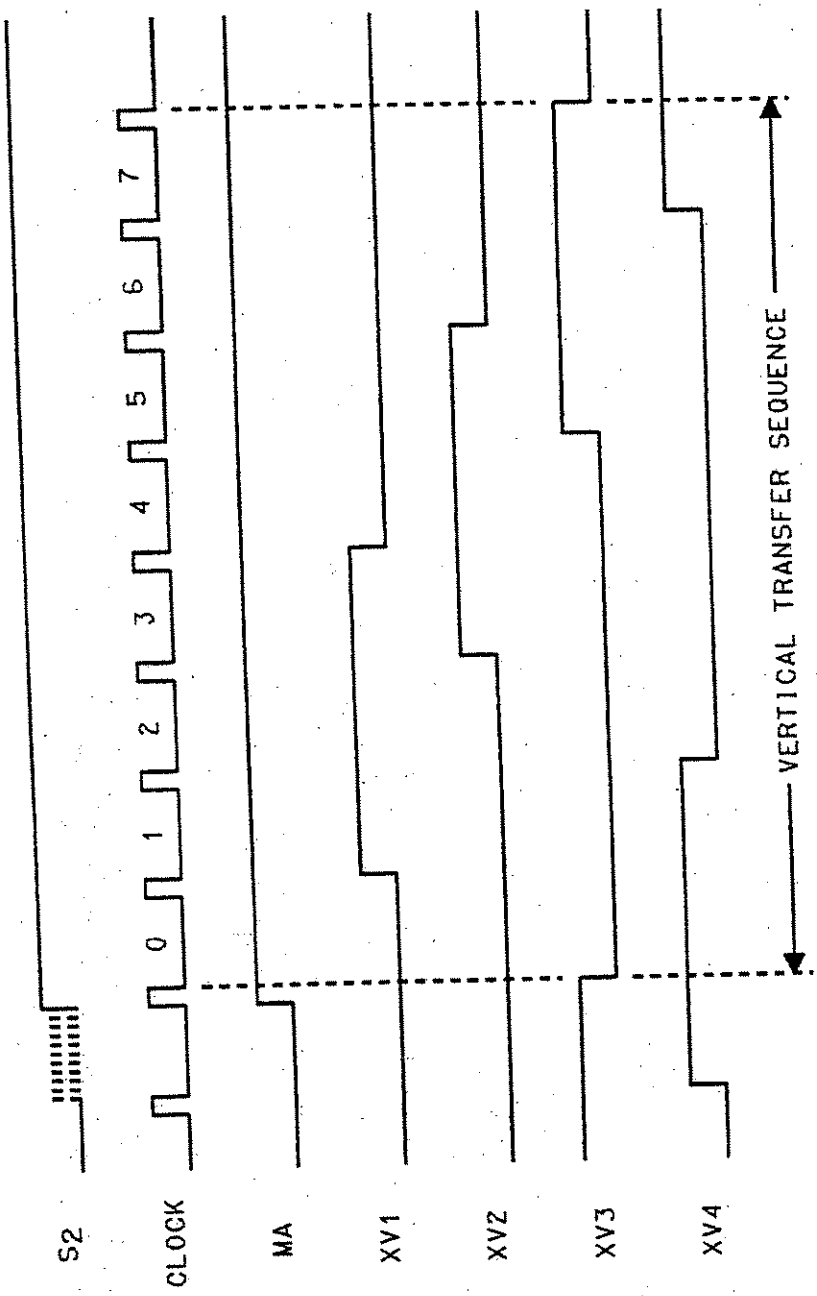

S2
CLOCK
MA
XV1
XV2
XV3
XV4
0
1
2
3
4
5
6
7
VERTICAL TRANSFER SEQUENCE

FIG. 5

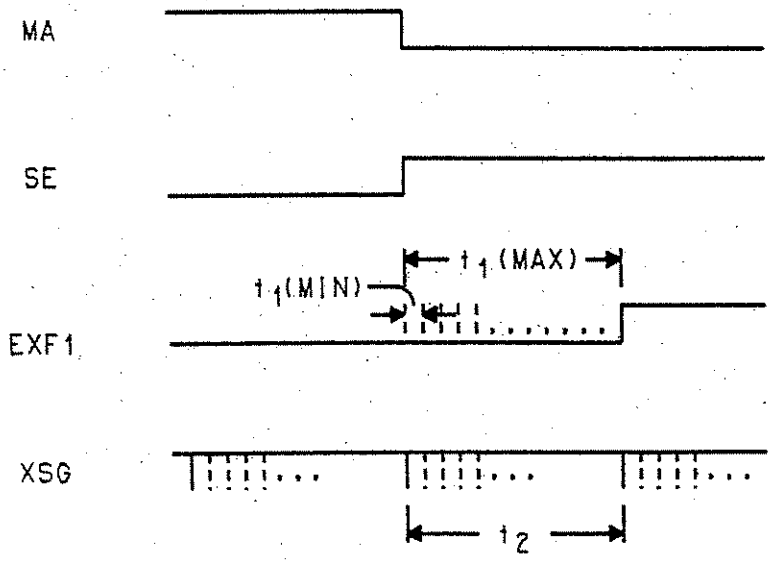


FIG. 6

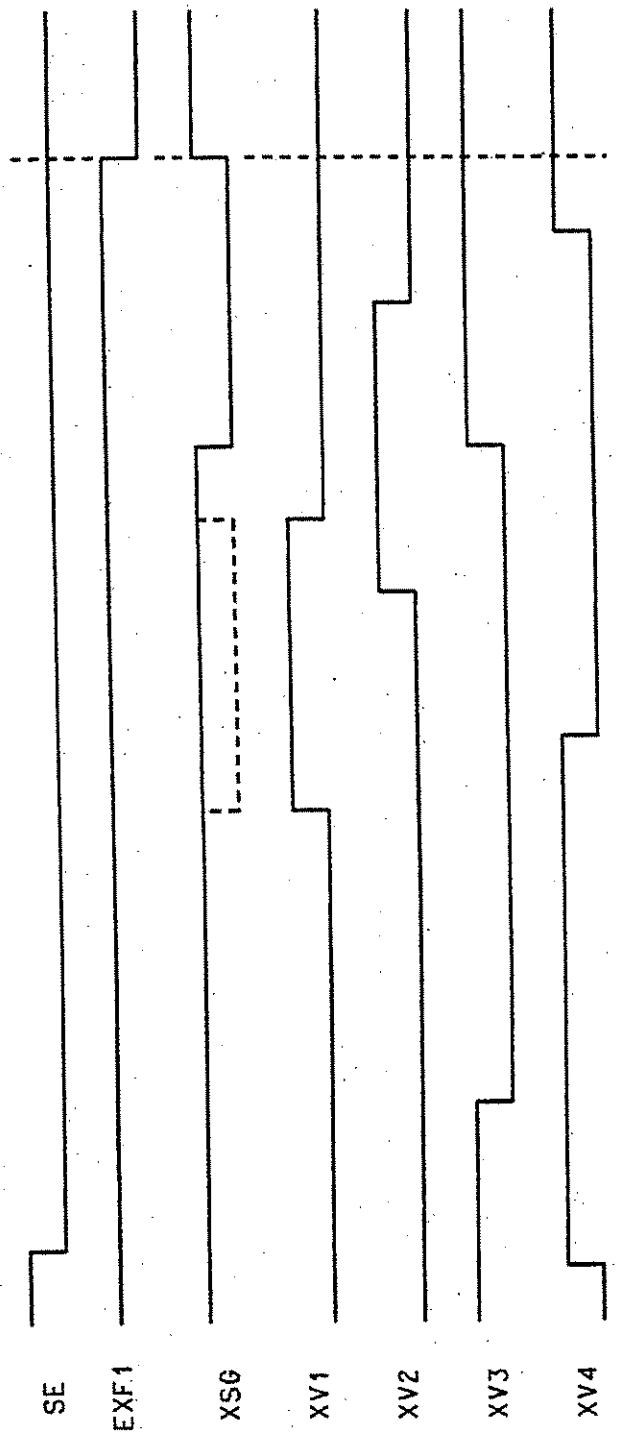


FIG. 7

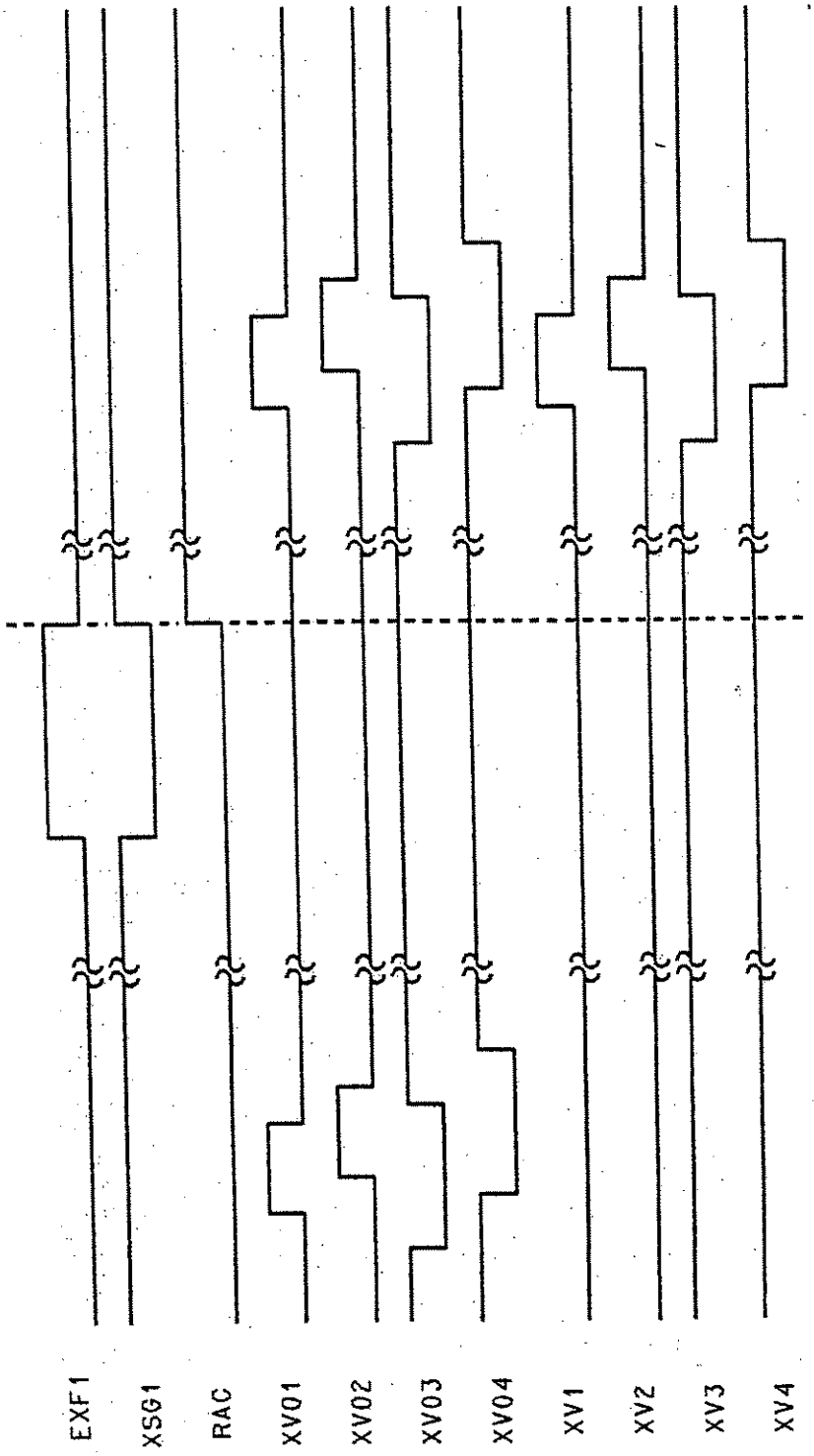


FIG. 8

AXD024486

ASYNCHRONOUS STILL TIMING FOR A VIDEO CAMERA PRODUCING MOVIE OR STILL IMAGES

CROSS REFERENCE TO A RELATED APPLICATION

This application is related to copending patent application Ser. No. 880,461, entitled "Exposure Control Apparatus for a Still Video Camera Having an Electronic Viewfinder", filed in the names of T. Nutting and R. Shroyer on June 30, 1986.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of still video imaging, and especially to the timing and control circuits of an image sensor for a still video camera of the type that produces a movie image in addition to a still image.

2. Description Relative to the Prior Art

A still video camera, by virtue of its inherent video processing capability, is well suited for combination with an electronic viewfinder (see, for example, the camera disclosed in U.S. Pat. No. 4,456,931). This combination is particularly advantageous for previewing the picture as it will actually appear subsequent to video processing. Such a camera operates in two modes: a movie mode for producing a moving video image in the viewfinder and a still mode for producing and recording a still image. The movie mode is comparable to the operation of any motion picture video camera. In such a camera, the photosensitive region of an image sensor is continuously irradiated by scene light. Since the exposure time is fixed to accord with the video image rate (e.g., 1/30th second), the image sensor is repetitively processed at a corresponding image frequency (e.g., 30 frames/second).

In the still mode, it is desirable that the exposure time is controlled so as to vary the length of time the image sensor is exposed to light. The image sensor must therefore be processed, not repetitively, but only once in a manner that defines the required exposure time and produces a video signal corresponding to the exposed image. Since a common image sensor is preferably the signal source for both modes, one mode excludes the other, that is, the movie mode can only precede, or follow, the still mode. This fact of operation leads to the conventional timing sequence in a still video camera. For instance, in U.S. Pat. No. 4,456,931, a control circuit is disclosed which either provides one set of drive signals to the image sensor when the monitor (viewfinder) displays the image focused on the image sensor or another set of drive signals to initiate and process the still exposure. Though not showing an electronic viewfinder like that shown in the preceding patent, U.S. Pat. No. 4,541,016 discloses a full-frame image pickup device that is synchronized, in its still operation, to a continuously running vertical drive signal. Since the charge storage period of each field is treated independently of the other, this disclosure suggests that a solid state image pickup unit equipped for still image pickup could also provide moving image pickup like an ordinary video camera.

Despite such suggestions from the prior art, it is not a trivial matter to incorporate movie timing with still timing. Substituting one set of drive signals . . . the still drive signals . . . for another set of drive signals . . . the movie drive signals . . . is not a totally asynchronous operation, as might be implied in U.S. Pat. No. 4,456,931. If for no other reason than cost, duplication of timing circuits is preferably avoided. More importantly, the two sets of drive signals must be tied together for the system to make a smooth transition from movie to still and back. On the other hand, if the still drive signals are totally synchronous with the vertical drive signal, as is the case in U.S. Pat. No. 4,541,016, the still exposure must occur in lockstep with the moving image pickup function. This is unfortunate in that the desired beginning of a still exposure seldom coincides with the beginning of the vertical drive interval. Some delay, i.e., up to 1/60 second, could thus be encountered before actually beginning the still exposure.

SUMMARY OF THE INVENTION

By initiating the still exposure in synchronism with the high frequency driving signals that operate an image sensor . . . instead of the vertical drive signal . . . a "pseudo"-asynchronous relationship can be obtained with the movie mode. True, the beginning of the still exposure is still in "lockstep" with a repetitive signal, but now with a signal that repeats in terms of nanoseconds (or microseconds), instead of milliseconds. The initiation of the still exposure thus becomes in effect "substantially" or "pseudo" asynchronous with respect to the image repetition frequency that governs the movie mode. The beginning of the still mode, i.e., the still exposure, becomes in a practical sense independent of the movie mode. Though the movie mode in the preferred embodiment is connected with the use of an electronic viewfinder, the invention relates more generally to the integration of a still exposure with any type of movie function, including the exposure and the recording of video movie images.

A still video camera according to the invention includes a signal generator for generating a continuous stream of imager driving signals for operating the image sensor according to a specific image repetition rate. A transfer circuit applies these imager driving signals to the image sensor when the image sensor operates as a signal source for a movie image. A still driving signal is also generated for operating the image sensor as a signal source for a still image. When an exposure release switch (for a still exposure) is actuated, the application of the imager driving signals to the image sensor is interrupted and the still signal is substituted therefor in synchronism with the imager driving signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described with reference to the drawings, in which:

FIG. 1 is a block diagram of a still video camera incorporating a timing and control circuit according to the invention;

FIG. 2 is an illustration of a conventional interline-transfer imaging device used in the camera of FIG. 1;

FIGS. 3 (A and B) is a rendition of the block diagram of FIG. 1 in further detail;

FIG. 4 is a timing diagram describing signal conditions during the operation of the camera shown by FIG. 3;

FIG. 5 is a detailed expansion of the beginning of still mode timing as shown by FIG. 4;

FIG. 6 is a detailed expansion of the beginning of the still exposure period as shown by FIG. 4;

FIG. 7 is a detailed expansion of the end of the still exposure period as shown by FIG. 4; and

FIG. 8 is a detailed expansion of the portion of FIG. 4 showing the return to the movie mode.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Because video cameras and video cameras employing electronic viewfinders are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIG. 1, the pertinent sections of a still video camera are shown for purposes of describing the invention: An optical section 10 directs image light to an image sensor 12, which in its preferred form is a conventional solid-state, interline-transfer image sensor. The basic elements of a conventional interline-transfer image sensor are shown schematically in an abbreviated form in FIG. 2. Briefly, the light gathered by the optical section 10 causes charge to collect in an array of photosites according to the pattern of the image. A group of imager driving signals (XSG, XV and SH) determine the operation of the sensor—in the case of a charge-coupled device, certain of these signals (XV and XH) prescribe a phase-related control of charge movement, hence the term phasing signals. When a transfer gate signal XSG is low, the image charge packets that have collected in the photosites transfer through a set of transfer gates to a corresponding set of vertical charge-coupled (CCD) shift registers. There a set of vertical phasing signals XV1 . . . XV4 transfer the charge packets to a horizontal CCD shift register, from which they are transferred off the image sensor by a horizontal phasing signal XH. Vertical and horizontal transfers are accomplished by biasing the registers with the respective phasing signals to form an array of independent potential wells, which are then shifted by varying the bias levels of the phasing signals in tandem.

Referring back to FIG. 1, a system controller 14, preferably a microprocessor, controls the general operation of the camera, including the optical section 10 and an exposure control circuit 16. A video signal generated by the image sensor 12 is converted into a line sequential color signal by a signal processing section 18. A monochrome rendition of the signal is displayed upon an electronic viewfinder 20 and, at the appropriate time, the color signal is prepared for recording in a record processing section 22. The recording signal is applied to a recording head 24 and recorded upon a magnetic disk 26. The disk 26 is mounted for rotation within a cartridge housing 28, which has an opening that allows the recording head 24 to contact the disk 26 for recording a plurality of concentric tracks (which correspond to a plurality of images). Finally, a timing circuit 30 synchronizes the signal processing section 18, the record processing section 22, and the viewfinder 20, with the image sensor 12. In particular, the timing circuit 30 produces the transfer gate signal XSG, and the phasing signals XV1 . . . XV4 and XH.

A number of additional signals are shown in FIG. 1, as follows: A moving aperture signal MA (from the controller 14 to the timing circuit 30) signifies that a shutter button has been pressed for a still exposure and that the optical aperture presented to incoming light is being adjusted by the optical section 10. A start exposure signal SE (from the controller 14 to the timing circuit 30) follows the signal MA and signifies that the aperture is correctly established and a still exposure can begin. An expose field signal EXF1 (from the timing circuit 30 to the controller 14) then indicates that the still exposure indeed has begun. A blanking signal BLK (from the controller 14 to the timing circuit 30) controls the blanking of the electronic viewfinder 20. The recording period is regulated by a record activate signal RAC (from the timing circuit 30 to the record processing section 22). Each of these signals will be further described in connection with FIGS. 3 and 4.

Referring to FIG. 3A, the optical section 10 includes a lens system 32 for directing image light from an object (not shown) to the image sensor 12 through a partially transmissive mirror 34 and a color filter 36. A diaphragm 38 regulates the optical aperture (through which image light passes) by a linkage with a diaphragm driver 40. The system controller 14 and the driver 40 communicate with one another on a line 42 when the aperture is to be, or has been, changed. When the camera is first energized, signals on the line 42 direct the driver 40 to drive the diaphragm 38 to an initial known point, such as fully open. After initialization, the system controller 14 continuously monitors, and saves, the aperture value of the diaphragm 38 by combining its previous known aperture setting with the newly calculated setting, as represented by the effect of the present signals being sent to the driver 40 over the line 42. The optical section 10 also interacts with the exposure control circuit 16, which receives a sample of image light diverted by the mirror 34. The exposure control circuit 16, which employs an integration cycle in its exposure determination process, includes a photodiode 44 and a light integrating circuit 46 that cooperate with a timing procedure (shown by a broken-line box 48) in the system controller 14 to arrive at a brightness value of the incoming image light. The light integrator 46 is enabled by the system controller 14 on a line 50*a*; when the integration cycle is complete, a signal is returned to the controller 14 on a line 50*b*.

The video signal generated by the image sensor 12 (by application of the aforementioned signals XSG, XV1 . . . XV4 and XH) is applied to a signal correction circuit 52, which performs a sample and hold operation and applies gain, white balance and gamma corrections to the signal. The color signal is applied to a matrix 54, which, in combination with a set 56 of 1H delay lines, produces a luminance (Y) signal, and a pair of color difference signals (B-Y, R-Y). The luminance signal is applied to a NTSC encoder 58 and a luma delay stage 60, the latter mainly to account for subsequent color delays in the modulation process. Meanwhile the color difference signals are put in line sequence by a chroma sequencer 62. The luminance signal is tapped at this point (see FIG. 3B) and directed through a monochrome (B/W) signal processing circuit 64 to the electronic viewfinder 20 (which is a conventional monochrome display). The viewfinder display is controlled by conventional vertical and horizontal sweep circuits 66.

The luminance signal and the color difference signals are input to a modulator 68, which provides a selected preemphasis to the input signals and frequency modulates a suitable set of carriers with the preemphasized signals. When permitted by the condition of the record activate signal RAC from the system timing circuit 30, the modulated signal is amplified by a head driver cir-

cuit 70 and applied to the recording head 24. The recording portion of the camera includes a disk drive motor 72 for rotating the magnetic disk 26 adjacent the recording head 24. The head 24 is moved by a stepper motor 74 that is connected to a stepper driver circuit 76 controlled from the system controller 14. The disk drive motor 72 is operated at a constant speed by a speed control circuit 78 coupled to the timing circuit 30.

The system timing circuit 30 and the system controller 14 are mutually adapted for the two modes of operation: movie and still. In the movie mode, the exposure time is fixed and the aperture is set to a value determined by the exposure control circuit 16 and the system controller 14. In the still mode, on the other hand, both exposure time and aperture may be varied. One of several conventional exposure modes is selected by designating a unique input to the system controller 14 on a line 80 for the type of mode: for example, aperture-preferred, shutter-preferred, manual, and one or more conventional program modes for emphasizing action photos, for emphasizing depth-of-field, for compromising somewhere between the two preceding modes, and so on. (Methods for calculating the exposure time and/or the aperture value according to these modes are well known from the conventional photographic arts.) Depending on the exposure mode in use, the exposure time and/or aperture value are manually entered to the system controller 14 on line(s) 82. The movie mode is initiated by partially depressing a two-position shutter button 84 to its first position, thereby setting a signal S_1 high. the still mode is subsequently selected when the shutter button 84 is fully depressed to its second position and an exposure release signal S_2 is set high.

The system control circuit 30 has a free-running circuit component in the form of a NTSC timing generator 86 and a movie timing generator 88, and an intermittently-operated component in the form of a still timing generator 90. The NTSC generator 86 provides a horizontal drive signal HD and a vertical drive signal VD according to NTSC standards. The movie timing generator 88 keys upon the drive signals from the NTSC timing generator 86 and generates a set of transfer gate signals XSG1 and XSG2 for the respective fields of a television frame and a set of four vertical register phasing signals XVϕ1 . . . XVϕ4 for operating the vertical registers of the image sensor (see FIG. 2). The movie timing generator 88 also provides the timing for the signal processing circuit 18, including sample and hold pulses for the signal correction section 52, clamping levels, and so on.

An imager clock generator 92 receives input signals from either the movie timing generator 88 or the still timing generator 90 and applies its output to a clock driver 94, which provides the phasing signals XSG, XV1 . . . XV4 and XH to the image sensor 12. The clock generator 92 serves, in the movie mode, as a conduit for the vertical phasing signals XVϕ1 . . . XVϕ4 by transferring them directly to the clock driver 94 and, in the still mode, as a generator of the still timing that defines the still exposure sequence. The field transfer gate signals XSG1 and XSG2 are combined in an OR function by the imager clock generator 92 and, in the movie mode, applied to the clock driver 94 as the transfer gate signal XSG seen in connection with FIG. 2. In the still mode, the XSG signal is independently generated in a preliminary sequence to clear the image sensor 12 of extraneous charge and then to define the still exposure period. Though the XSG signal is shown in FIGS. 1, 2, and 3A as being separately applied to the transfer gates of the image sensor 12, in the preferred embodiment the XSG signal is instead presented as a higher than usual bias level on one of the vertical phasing signals at the moment a transfer is called for; the result . . . the transfer of image charge to the vertical registers . . . is the same for either technique. The imager clock generator 92 and the still timing generator 90, though shown as functionally separate in FIG. 3A, may be combined in one circuit component, such as a programmable logic sequencer.

Referring to FIG. 4 in connection with FIGS. 3A and 3B, when the movie mode is initiated by setting the signal S_1 high, the blanking signal BLK from the system controller 14 to the movie timing generator 88 is set low. The movie timing generator 88 accordingly permits the signal processing circuit 18 to pass a video signal to the viewfinder 20. In the movie mode, the timing circuit 30 produces the vertical transfer gate signal XSG for opening the transfer gates of the image sensor according to the vertical drive frequency. Vertical register phasing signals XV1 . . . XV4 and horizontal register phasing signals XH (not shown in FIG. 4) remove the video signal from the image sensor within each field period, applying it to the signal processing section 18 to generate a conventional monochrome video movie display in the viewfinder 20. Meanwhile, the integration period of the exposure control circuit 16 is initiated by a signal on the line 50α and continues until the output of the integrator 46 reaches the level of a reference voltage. For example, the reference voltage is set to correspond to an (average) integration time of 5 milliseconds which, for an average exposure, permits a rapid evaluation of the brightness of the incoming image light . . . in particular, more rapid than the field rate as shown by the vertical drive frequency. Each integration period is measured by the software timer 48 and the actual brightness is determined by the time deviation from an average exposure. Another integration period begins after this one is terminated, and another after the next is terminated, and so on, to form the integration cycle characteristic of the movie mode. An explanation of this integration cycle, which is unnecessary for an understanding of the present invention, can be found in further detail in copending Ser. No. 880,461

The vertical drive signal shown in FIG. 4 determines the video rate for the movie mode of operation. The still mode of operation can be seen from the subsequent waveforms as an interruption of the movie video rate; in particular, both a preliminary sequence of aperture adjustment/sensor clearing and the actual still exposure can be commenced without regard to the vertical drive. The the still mode is initiated in relation to the clock period governing the phase signals XV1 . . . XV4. This clock signal is seen in FIG. 5 as a separate signal that determines the edge transitions of the phasing signals XV1 . . . XV4. The vertical transfer sequence (the time for a potential well to move one increment) is determined by 8 periods of the clock. The signal MA, which begins the still mode sequence, is only recognized on a transition of the clock signal. (The signal MA may in practice be as short as, say, 70 microseconds; it is shown relatively elongated in FIG. 4 for ease of illustration only). Since, in the preferred embodiment, each clock period is 489 nanoseconds, the onset of the signal MA will follow the rising edge of the signal S_2 by no more than 489 nanoseconds. (If the exposure release signal S_2

went high during a field transfer pulse XSG1 or XSG2, an additional 20 microseconds are allowed before the onset of the signal MA). Nonetheless, the total effective delay is so small as to be negligible to the human user of the camera and, indeed, to the picture-taking function of the camera itself.

With the onset of the signal MA, the signal BLK is set high and the movie timing generator **88** accordingly directs the signal processing circuit **18** to clamp its output signal to a black level. This effectively blanks the viewfinder **40**. The system controller **14** issues signals on the line **42** to move the diaphragm to its still aperture value, which was predetermined by operation of the exposure control circuit **16** (see copending Ser. No. 880,461, for more detail). In the meantime the still timing generator **90** has interrupted the imager clock generator **92** and has initiated a rapid-fire sequence of XSG pulses to the transfer gates of the image sensor **12** to clear the photosites of extraneous unwanted charge. From there the charge is cleared by rapid operation of the vertical and horizontal registers. In this connection, the vertical phasing signals XV1 . . . XV4 shown by FIG. **5** begin a rapid sequence in which the vertical transfer sequence is considerably shortened, say to 3.9 microseconds, so that each full clearing sequence lasts 1 millisecond. When the aperture is set, a start exposure signal SE can be sent to the timing circuit **30** to indicate that an exposure should commence.

FIG. **6** is a detailed view of the relationship of the start exposure signal SE to the clearing sequence t_2. Depending on when the signal XSG is pulsed low, a short time interval $t_1$elapses before the next clearing sequence is completed following receipt of the signal SE. This time ranges from one clock cycle (**489** nanoseconds) to a full clearing sequence (1 millisecond). The time interval t_1 terminates with the system timing circuit **30** momentarily dropping the gate signal XSG low one more time to open the image sensor transfer gates. As soon as the transfer gates are closed (XGS is high), the image sensor photosites immediately begin to collect charge from the incident image light and the still exposure period begins. Simultaneously, the timing circuit **30** notifies the system controller **14** with the expose field signal EXF1 that the still exposure has begun. Since there is non-image charge residing in the vertical registers, the phasing signals XV1 . . . XV4 are sequenced one more time (at the fast rate) until the vertical registers are fully cleared.

While the signal MA is high the signal on the line **50***a* is set low so that the exposure circuit **16** does not operate during the pre-exposure clearing sequence. At the instant the expose field signal EXF1 goes high, the signal on the line **50***a* likewise goes high, thereby beginning the still exposure control integration cycle in synchronism with the still image exposure cycle. The reference voltage provided to the integrator **46** for the still integration cycle is related to the overall exposure required of the image sensor **12** in the still mode. When the integrated voltage equals the level of the reference voltage, the signal on the line **50***b* changes state, thus notifying the system controller **14** that the exposure should end (the software timer **48** is not used in the still mode). The system controller **14** notifies the timing circuit **30** that the exposure should end by driving the start exposure signal SE low. The transfer gate signal XSG drops low thereby transferring the integrated image charge from the photosites to the vertical registers. Since the vertical registers in a conventional interline-transfer device are light-protected by an opaque coating, the image charge is light-protected and the still exposure is terminated. In this connection, it is noteworthy that the clearing sequence t_2 is set, in time, to correspond to the fastest exposure time demanded of the camera, i.e., one millisecond, thus insuring that the image charge transfer into the vertical registers never occurs before all extraneous charge is removed therefrom. Though this particular transfer techniques is not essential to the practice of the invention, it is also noteworthy that the use of the vertical registers for charge storage prescribes a camera that processes and records a single video field, rather than a frame.

As shown by FIG. **7**, the transfer of the image charge occurs in relation to a transfer sequence of the phasing signals XV1 . . . XV4 (which have been static since the last field of extraneous charge was dumped after the still exposure was started). It is necessary for the phases of the vertical phasing signals XV1 . . . XV4 to be in a particular state for the transfer back to the movie mode to later occur, as follows:

XV1=low
XV2=low
XV3=high
XV4=high

This phase condition occurs after the lapse of a single vertical transfer sequence (in correspondence with the broken line to the left of FIG. **7**). During this sequence, one of the two video fields is transferred . . . as shown by either the solid-line pulse or the broken-line pulse in the XSG signal (FIG. **7**). The expose field signal EXF1 then drops low, indicating to the system controller **14** that the exposure is over. (The exposure period, i.e., the time that the signal EXF1 is high, is shown to be relatively long in FIG. **4** . . . almost a whole field; in practice, it can be as short as 1 millisecond).

These conditions remain static until the next occurrence of the XSG1 or XSG2 pulse. For this pulse, the transfer gate signal XSG is inhibited since the meaningful image charge in the vertical registers must not be contaminated by residual charge that has accumulated in the photosites since the exposure ended. The transfer of control from the still mode to the movie mode takes place at this time and is shown in more detail in FIG. **8**. The vertical transfer clock signals XVϕ1 . . . XVϕ4 have been temporarily interrupted by the imager clock generator **92**, which substituted the timing instructions received from the still timing generator **90**. Due to the phase synchronization done at the end of the still exposure (see FIG. **7**), the vertical transfer clock signals XV1 . . . XV4 are presently in the static state shown to the left of the broken line dividing FIG. **8**. When the signal XSG1 (or XSG2) is first pulsed low by the movie timing generator **88** after the signal SE has dropped low, the transfer of control is obtained, i.e., the vertical clock signals XV1 . . . XV4 are resynchronized to the clock signals XVϕ1 . . . XVϕ4 from the movie timing generator **88**. The transfer occurs as shown by FIG. **8** for the signal XSG1; if the signal XSG2 occurs first, the transfer occurs slightly later due to the relative positions of the vertical phasing signals.

Since the signal processing section **18** is driven by the movie timing generator **88** in either mode, the video information is clocked off the imager **12** and processed into a video signal by the circuits making up the section **18**. Meanwhile, the concurrence of a XSG1 (or XSG2) pulse and an EXF1 pulse activates a record logic section **87** in the timing circuit **30**. The record activate

signal RAC is thus set high, which activates the head driver 70, and the still video signal is recorded on the magnetic disk 26. At the occurrence of the next vertical drive interval the transfer gate signal XSG resumes its movie mode of operation and a movie image is displayed on the viewfinder 20, i.e., the signal BLK is set low. (Since the first two fields taken from the image sensor after a still exposure may be over or underexposed due to the continuance of still exposure conditions, it may be preferable to continue blanking the viewfinder 20 for these two fields).

FIG. 4 shows the period from the initiation of the still mode to the beginning of the still exposure as extending over a substantial portion of the vertical drive interval. This is shown mainly for purposes of illustration, since much is happening during this period. In practice, the period may be as short as the system can recognize and utilize. In the preferred embodiment as little as 70 microseconds are allocated to this period (the high state of the signal MA) if the aperture needs no adjustment. Small aperture adjustments require somewhat more time, larger adjustments yet greater time. The origination of the signal MA is keyed to the exposure release signal S_2. In certain situations, it may be desirable to allow some time between the signal $S_2$and the onset of the signal MA. For instance, the controller 14 might not drive the signal MA high until the presently running exposure integration cycle is completed. This feature, described in connection with the cross-referenced copending Ser. No. 880,461, is an optional practice that is unessential to practice of the present invention. Even if used, the benefits of the present invention are obtained since the movie integration cycle is set to occur in less than the time of the vertical interval. Moreover, the onset of the still mode is still initiated in synchronism with the clock period of the phasing signals that drives the image sensor, i.e., it is asynchronous with respect to the vertical drive interval.

The disclosure thus far has been of an "electronically-shuttered" camera, i.e., a camera without a mechanical shutter. If a mechanical shutter is provided, it would preferably be closed at some point after initiation of the still mode and then opened during the still exposure period (when the signal EXF1 is set high). For instance, referring to the waveform for the signal EXF1 in FIG. 4, the mechanical shutter (not shown separately) would be opened during a period t_s, which is shown to extend in time from an arrow A to an arrow B comprising a portion of the high cycle of the signal EXF1. The exposure control circuit 16 would be accordingly keyed to the period t_s so as to properly determine the exposure. Using a mechanical shutter means that the light-protected vertical registers on the image sensor 12 would not have to be used to protect the image charge. A full-frame exposure could therefore be made and, while the shutter is closed, each field could be separately clocked off the image sensor 12. The initiation of the still mode and the still exposure period would continue to maintain their asynchronous relation to the vertical drive interval, as heretofore disclosed.

The foregoing disclosure describes a still video camera that maintains the necessary timing synchronization between the movie mode and the still mode of operation without having to delay a still exposure just to "catch up" to some slowly (relatively) running movie reference. By synchronizing the "change-over" to the still mode, and the beginning of the still exposure, to the cyclical character of the image sensor clock signals, rather than to the image repetition frequency, the onset of a still exposure can be made to appear, due to the short times involved, asynchronous with respect to the movie mode. In other words, the camera can, without delay, record a still rendition of the observed scene when the shutter button is pressed.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention. For example, the camera has been especially set up to operate according to NTSC television standards, but it is clear that, with a suitable image sensor and readily implemented changes in the timing circuits, PAL or SECAM standards could be accommodated as well.

What is claimed is:

1. A still video camera of the type having an image sensor that generates a charge pattern in response to image light from an object and operates thereupon either as a signal source for a movie image, according to a specific image repetition rate, or as a signal source for a still image, the camera further including a release switch for initiating a still exposure period, said camera comprising:

means for generating a continuous stream of movie phasing signals for operating upon the charge in the image sensor at a rate that is substantially greater than the image repetition rate;

transfer means for applying said movie phasing signals to the image sensor when the image sensor operates as a signal source for a movie image;

means for generating a still phasing signal for operating the image sensor as a signal source for a still image; and

means responsive to actuation of the release switch for interrupting the application of said movie phasing signals to the image sensor and for substituting therefor said still phasing signal synchronously with respect to said movie phasing signals and asynchronously with respect to said image repetition rate.

2. The camera as claimed in claim 1 further including:

means for generating an end exposure signal at the end of the still exposure period; and

means responsive to said end exposure signal for directing said transfer means to resume application of said movie phasing signals to the image sensor.

3. The camera as claimed in claim 2 in which said movie phasing signals are resumed in synchronism with the image repetition rate.

4. The camera as claimed in claim 3 in which said image sensor is of the type that has one or more light-protected storage elements for temporarily storing the image-wise charge pattern until it can be removed from the sensor, said movie phasing signal generating means initiating the transfer of charge to the storage elements at an image repetition rate corresponding to field intervals, said still phasing signal generating means initiating the transfer of image charge to the storage elements after the end of the still exposure period, and said means responsive to said end exposure signal resuming application of said movie phasing signals at the beginning of a subsequent field interval.

5. A still video camera of the type that includes an electronic viewfinder for previewing a video image of an object and an image sensor that generates a charge pattern in response to image light from the object, said

image sensor operating either as a signal source for the viewfinder according to a specific image repetition rate or as a signal source for a still image processed by the camera, the camera further including a diaphragm for regulating the aperture presented to the image light and a release switch for initiating a still exposure period, said camera comprising:

means for generating a continuous stream of movie phasing signals for operating the image sensor according to a specific frequency multiple of the image repetition rate;

means for generating at least one still phasing signal for operating the image sensor as a signal source for a still image;

transfer means for applying either said movie or said still phasing signals to the image sensor when the image sensor operates respectively as a signal source for either the viewfinder or for a still image;

means responsive to actuation of the release switch and initiated in synchronism with said movie phasing signals for setting the diaphragm to a predetermined still aperture;

means responsive to said still phasing signal and to the setting of said predetermined still aperture for initiating the still exposure period;

means for generating an end exposure signal at the end of the still exposure period; and

means responsive to said end exposure signal for triggering said transfer means to resume application of said movie phasing signals to the image sensor.

6. The camera as claimed in claim **5** in which said transfer means resumes application of said movie phasing signals to the image sensor in synchronism with the image repetition rate.

7. The camera as claimed in claim **6** in which said image repetition rate corresponds to a video field frequency and said transfer means resumes application of said movie phasing signals to the image sensor in synchronism with the beginning of a video field.

8. A still video camera of the type that includes an electronic viewfinder for previewing a video image of an object and a clocked image sensor having charge-generating photosites and at least one charge-coupled register for transferring image charge from the photosites, said image sensor operating upon the image charge either as a signal source for the viewfinder or as a signal source for a still image processed by the camera, the camera further including a diaphragm for regulating the aperture presented to image light and a release switch for initiating a still exposure period, said camera comprising:

means for generating a high frequency clock signal for operating upon the image charge in the sensor;

movie timing means responsive to said clock signal for generating a low frequency movie driving signal for moving image charge from the photosites of the image sensor to the register in correspondence with a specific image repetition frequency;

still timing means responsive to said clock signal for generating a still driving signal for operating the image sensor during the still exposure period;

control means for engaging either said movie timing means or said still timing means in the operation of the image sensor, said control means having a preview state in which said movie driving signal is passed to the image sensor and a still exposure state in which said still driving signal is passed to the image sensor;

means responsive to actuation of said release switch for engaging said control means in its still exposure state so that control of the image sensor in its still exposure state is initiated in time-dependent relation to the clock period of said clock signal and in substantial time-independent relation to the image repetition frequency;

means for generating an end exposure signal at the end of the still exposure period; and

means responsive to said end exposure signal for reengaging said control means in its preview state in time-dependent relation to the image repetition frequency, thereby returning control of the image sensor to said movie timing means.

9. A still video camera that includes an electronic viewfinder for previewing a video image of an object before a still image is processed by the camera, said still video camera comprising:

means for generating a high frequency clock signal;

movie timing means for generating a movie driving signal that is a frequency submultiple of said clock signal;

still timing means for generating a still driving signal that regulates the length of the still exposure;

an image sensor that receives image light from the object and generates a sensor signal therefrom, said image sensor being (a) under control of said movie timing means when operated as a signal source for the viewfinder, said movie driving signal initiating the removal of the sensor signal from said image sensor at set video intervals according to said movie driving signal, and (b) under control of said still timing means when operated as a signal source for the still image;

an exposure release switch for initiating a still exposure;

means responsive to initiation of a still exposure for transferring control of said image sensor from said movie timing means to said still timing means in time-related synchronism with respect to said clocking signal; and

means responsive to the end of the still exposure for transferring control of the image sensor back to the movie timing means in time-related synchronism with respect to said movie driving signal.

10. The camera as claimed in claim **9** further including:

a diaphragm for regulating the optical aperture of said image sensor to the image light and wherein said still timing means initially provides a diaphragm-adjusting signal to said diaphragm for setting a predetermined still aperture.

11. The camera as claimed in claim **10** further including:

means responsive to the termination of said diaphragm adjusting signal for beginning the still exposure of the image sensor.

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